7I78 STEP/DIR PLUS I/O DAUGHTERCARD

V1.2

Table of Contents

GENERAL

DESCRIPTION

The 7I78 daughtercard/breakout board for use with MESA's 25 pin I/O FPGA cards like the 5I25. The 7I78 is designed for interfacing up to 4 Axis of step&dir step motor or servo motor drives and also provides a spindle encoder interface, and an isolated analog spindle control.

All step and direction outputs are buffered 5V signals that can drive 24 mA. All outputs support differential mode to reduce susceptibility to noise.

One RS-422 interface is provided for I/O expansion via a serial I/O daughtercard. All field wiring is terminated in pluggable 3.5 mm screw terminal blocks.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I78 card is oriented in an upright position, that is, with the host interface DB25 connector pointing towards the left.

CABLE 5V POWER

The 7I78 can get its 5V encoder, step/dir and serial interface power from the host interface card if desired. W1 determines if the 7I78 gets this 5V power from the host FPGA card. If W1 is in the left hand position, host cable power is used. If W1 is in the right hand position, 5V power must be supplied to the 7I78 and the 7I78 grounds the 4 DB25 signals used for host 5V power. This option must be set to match the cable power option of the host FPGA card. If the FPGA card supplies 5V, W1 must be in the left hand position. If the FPGA card does not supply 5V, W1 must be in the right hand position.

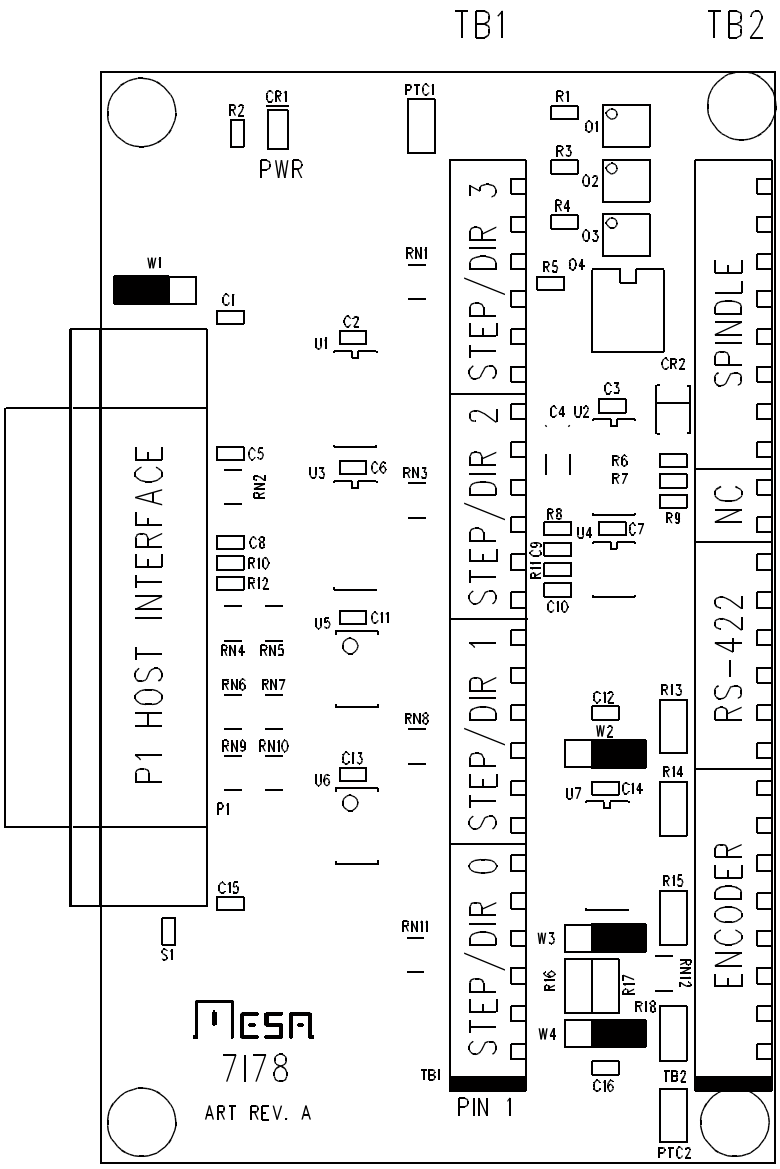
ENCODER INPUT MODE

The 7I78s encoder input can be programmed for differential or single ended mode operation. W2,W3 and W4 set the encoder input mode. When W2,W3,and W4 are in the right hand position, the encoder input is mode is differential. When W2,W3, and W4 are in the left hand position, the encoder input mode is single ended or "TTL".

Normally these jumpers would be all moved to the left or right hand positions as a group, but it is possible to change the input modes of the A/B/Z inputs individually. W2 controls the "Z" or index input mode, W3 controls the "B" input mode and W4 controls the "A" input mode.

CONNECTORS

7I78 CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

P1 HOST INTERFACE CONNECTOR

P1 is the DB25F connector on the 7I78 that connects to the FPGA card. Actual pin functions depend on FPGA configuration but signal directions must be observed.

DB25 PIN	GPIO	FUNCT	DIR	DB25 PIN	GPIO	FUNC	DIR
1	IO0	DIR0	OUT	14	IO1	STEP0	OUT
2	IO2	DIR1	OUT	15	IO3	STEP1	OUT
3	IO4	DIR2	OUT	16	IO5	STEP2	OUT
4	IO6	DIR3	OUT	17	IO7	STEP3	OUT
5	IO8	/SPINPWM	OUT	18	GND		
6	IO9	/SPINENA	OUT	19	GND		
7	IO10	SPINDIR	OUT	20	GND		
8	IO11	SSTX	OUT	21	GND		
9	IO12	/SSTXEN	OUT	22	GND or 5V		
10	IO13	SSRX	IN	23	GND or 5V		
11	IO14	QUADI	IN	24	GND or 5V		
12	IO15	QUADB	IN	25	GND or 5V		
13	IO16	QUADA	IN				

Notes:

1. If jumper W1 is is the left hand position, pins 22 through 25 are 5V, if W1 is in the right hand position, Pins 22 through 25 are GND.

2. GPIO pins are for first FPGA connector, next connector series begins at GPIO17

3. Signal directions are relative to FPGA card, that is, an ‘OUT’ signal is an output from the FPGA card that drives the 7I78. Conversely an ‘IN’ signal is a FPGA input that is driven by the 7I78.

CONNECTORS

TB1 STEP AND DIR CONNECTOR

TB1 is the 7I78s step and direction output connector. Both polarities of step and direction signals are provided. Each channel on the interface uses 6 pins. TB1 is a 3.5 MM pluggable terminal block with supplied removable screw terminal plugs.

TB1 CONNECTOR PINOUT

TB1 PIN	SIGNAL	TB1 PIN	SIGNAL
1	GND	13	GND
2	STEP0-	14	STEP2-
3	STEP0+	15	STEP2+
4	DIR0-	16	DIR2-
5	DIR0+	17	DIR2+
6	+5VP	18	+5VP
7	GND	19	GND
8	STEP1-	20	STEP3-
9	STEP1+	21	STEP3+
10	DIR1-	22	DIR3-
11	DIR1+	23	DIR3+
12	+5VP	24	+5VP

Note: 5VP pins are PTC short circuit protected 5V output pins for field wring

CONNECTORS

TB2 ENCODER, RS-422 AND SPINDLE CONNECTOR

TB2 has a mix of signals including analog spindle interface, an encoder interface, a RS-422 interface, and 5V power supply terminals TB3 is a 24 terminal 3.5 MM pluggable terminal block with supplied removable screw terminal plugs.

TB2 CONNECTOR PINOUT

TB2 PIN	SIGNAL	TB2 PIN	SIGNAL
1	ENCA+	13	RS-422 TX-
2	ENCA-	14	+5VP
3	GND	15	NC
4	ENCB+	16	NC
5	ENCB-	17	SPINDLE-
6	+5VP	18	SPINDLE OUT
7	IDX+	19	SPINDLE+
8	IDX-	20	NC
9	GND	21	SPINDLE ENA-
10	RS-422 RX+	22	SPINDLE ENA+
11	RS-422 RX-	23	SPINDLE DIR-
12	RS-422 TX+	24	SPINDLE DIR+

Note: 5VP pins are PTC short circuit protected 5V output pins for field wring.

OPERATION

HOST INTERFACE

The 7I78 is intended to operate with a FPGA card with parallel port pinout like the Mesa 5I25 or 6I25. The FPGA card supports the step/dir, encoder, PWM an GPIO for the spindle interface and smart serial interface for the expansion RS-422 port. The FPGA card can also supply 5V power to the 7I78.

STEP/DIR INTERFACE

The 7I78 provides 4 channels of step/dir interface with buffered 5V differential signals. The differential signals allows reliable signal transmission in noisy environments. If single ended drive is required, a single output of the differential pair may be used.

RS-422 INTERFACE

The 7I78 has one RS-422 interface available on TB2. This interface is intended for I/O expansion with Mesa SSERIAL devices. The easiest way to make a cable for interfacing the 7I78 to these devices is to take a standard CAT5 or CAT6 cable, cut it in half, and wire the individual wires to the 7I78 screw terminals. The following chart gives the CAT5 to 7I78 screw terminal connections (EIA/TIA 568B colors shown):

TB3 PIN	7I78 SIGNAL	DIRECTION	CAT5 PINS	CAT5 568B COLOR
15	GND	FROM 7I78	4,5	BLUE / WHITE
16	RX+	TO 7I78	6	GREEN
17	RX-	TO 7I78	3	GREEN / WHITE
18	TX+	FROM 7I78	2	ORANGE
19	TX-	FROM 7I78	1	ORANGE / WHITE
20	+5V	FROM 7I78	7,8	BROWN / WHITE

OPERATION

ENCODER INTERFACE

The 7I78 provide a one channel encoder interface with index. This is intended as a spindle encoder but can be used for other purposes. The encoder input can be programmed for differential or single ended encoders. The encoder interface also provides short circuit protected 5V power to the encoder. When used with single ended encoders, the ENCA+, ENCB+ and IDX+ signals are wired to the encoder and the ENCA-,ENCB-, and IDX- terminal left unconnected.

SPINDLE INTERFACE

The 7I78 provides one analog output for spindle control. The analog output is a isolated potentiometer replacement type device. It functions like a potentiometer with SPINDLE + being one end of the potentiometer, SPINDLE OUT being the wiper and SPINDLE- being the other end. The voltage on SPINDLE OUT can be set to any voltage between SPINDLE- and SPINDLE+. Polarity and voltage range must always be observed for proper operation. The voltage supplied between SPINDLE+ and SPINDLE- must be between 5VDC an 15VDC with SPINDLE + always being more positive than SPINDLE-.

Because the analog output is isolated, bipolar output is possible, for example with SPINDLE+ connected to 5V and SPINDLE- connected to -5V, a +-5V analog output range is created. In this case the spindle output must be offset so that 50% of full scale is output when a 0V output is required. Note that if bipolar output is used, the output will be forced to SPINDLE- at startup or when SPINENA is false.

Spindle PWM is active low so if the 7I78 is used with HostMot2 firmware, the PWM output must be inverted.

SPINDLE ISOLATED OUTPUTS

The 7I78 provides 2 isolated outputs for use for spindle direction control, and spindle enable. These outputs are OPTO coupler Darlington transistors. They are all isolated from one another so can be used for pull up or pull-down individually. They will switch a maximum of 50 mA at 0 to 100 VDC. The SPINDLE ENA output is special as it uses the same signal that enables the analog output. When the analog output is enabled, the SPINDLE ENA OPTO output is on.

REFERENCE INFORMATION

SPECIFICATIONS

	MIN	MAX	NOTES
GENERAL			
HOST SUPPLY VOLTAGE 5V	4.5 VDC	5.5 VDC	
5V CURRENT	----	100 mA	No ext load.
STEP/DIR OUTPUTS			
STEP/DIR OUTPUT HIGH V	4V	----	10 mA source
STEP/DIR OUTPUT LOW V	----	1V	10mA sink
ENCODER INPUT			
INPUT COMMON MODE RANGE	-7	+12	Volts
INPUT TTL MODE THRESHOLD	1.4	1.8	Volts
DIFFERENTIAL MODE IMPEDANCE	131	135	Ohms
COUNT RATE	----	10 MHz	

SPECIFICATIONS

RS-422 INTERFACE

MAXIMUM DATA RATE		----	10	MBIT/S
INPUT COMMON MODE RANGE		-7	+12	Volts
INPUT TERMINATION RESISTOR		131	135	Ohm
OUTPUT LOW	(24 mA sink)	----	.8	Volts
OUTPUT HIGH	(24 mA source)	VCC-.8	----	Volts

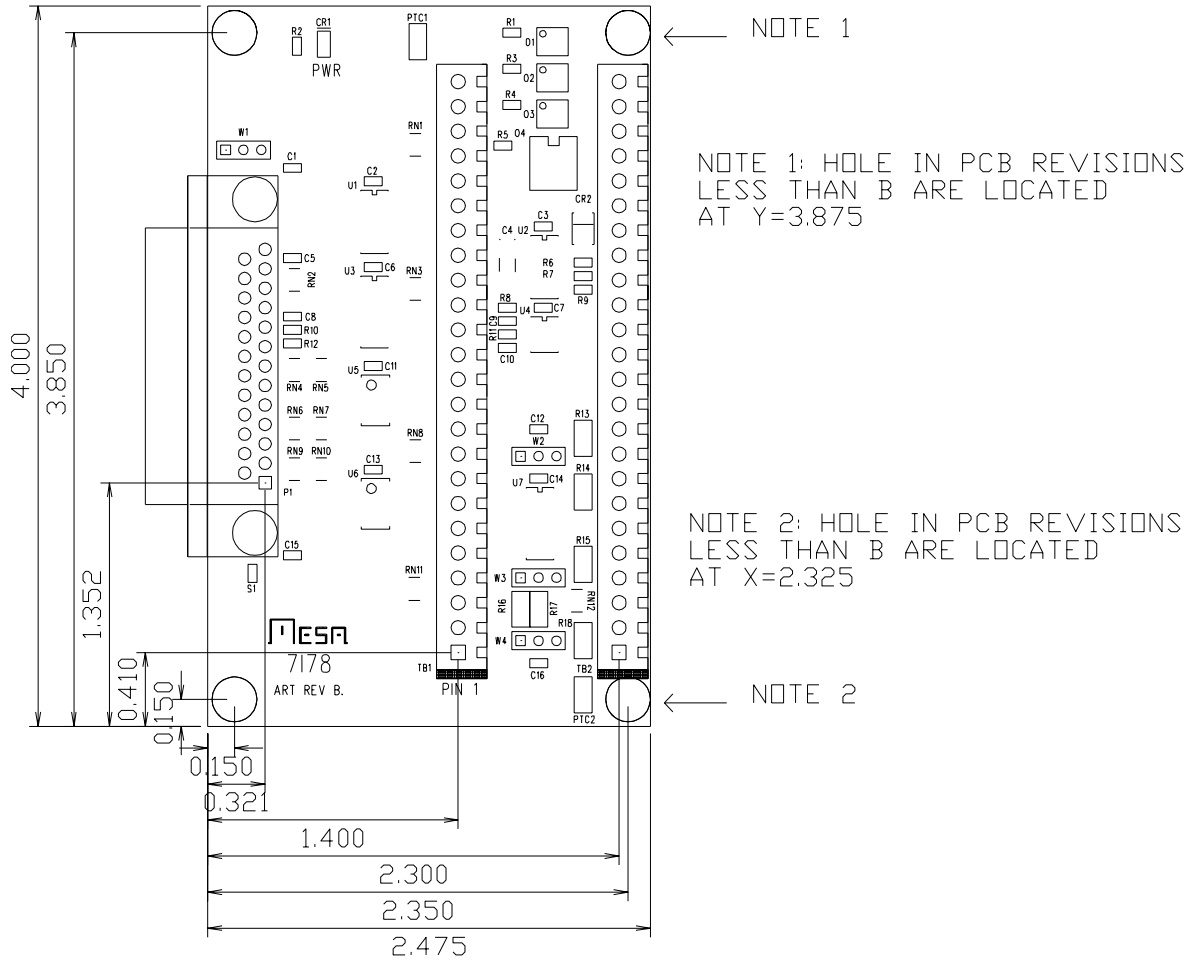
SPINDLE INTERFACE

REFERENCE VOLTAGE	5	15	Volts
(SPINDLE+ –> SPINDLE-)			
SUPPLY CURRENT	----	20	mA
ISOLATION VOLTAGE	----	500	Volts DC
NON-LINEARITY	----	1	% at 5KHz
DIR/ENA OUTPUT CURRENT	----	50	mA
DIR/ENA OUTPUT VOLTAGE	----	100	Volts DC
DIR/ENA ISOLATION VOLTAGE	----	500	Volts DC

ENVIRONMENTAL

TEMPERATURE -C VERSION	$0^{o}C$	$70^{o}C$
TEMPERATURE -I VERSION	$-40^{o}C$	$85^{o}C$

DRAWINGS


NOTE 1
NOTE 1: HOLE IN PCB REVISIONS LESS THAN B ARE LOCATED AT Y=3.875
NOTE 2: HOLE IN PCB REVISIONS LESS THAN B ARE LOCATED AT X=2.325
NOTE 2
4.000
3.850
1.352
0.410
0.150
0.150
0.321
1.400
2.300
2.350
2.475
PWR
7I78
ART REV B.
PIN 1