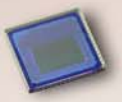
OmniVision



datasheet

PRODUCT SPECIFICATION

1/4" CMOS QXGA (3 megapixel) image sensor
with OmniPixel3™ technology

OV3640

color CMOS QXGA (3 megapixel) image sensor with OmniPixel3™ technology

datasheet (CSP2)
PRODUCT SPECIFICATION

version 2.21
october 2008

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still cameras

ordering information

- **OV03640-V56A** (color, lead-free)
  56-pin CSP2

features

- ultra low power and low cost
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, scaling, cropping, windowing, and panning
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555/444, YUV422/420, YCbCr422, and compression
- support for images sizes: QXGA, and any arbitrary size scaling down from QXGA
- support for video or snapshot operations
- support for horizontal and vertical sub-sampling
- support for data compression output
- support for auto focus control (AFC)
- support for anti-shake
- support for internal and external frame synchronization
- support for LED and flash strobe mode
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- MIPI serial output interface
- support for second camera chip-sharing ISP and MIPI interface
- embedded microcontroller
- embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- programmable I/O drive capability

key specifications

- **active array size:** 2048 x 1536
- **power supply:**
  core: 1.5VDC ± 5%
  analog: 2.5 ~ 3.0V
  I/O: 1.7 ~ 3.0V (1.8V is strongly recommended)
- **power requirements:**
  active: 75 mA (without MIPI)
  standby: 20 µA
- **temperature range:**
  operating: -20°C to 70°C (see **table 8-1**)
  stable image: 0°C to 50°C (see **table 8-1**)
- **output formats (8-bit):** YUV(422/420) / YCbCr422, RGB565/555/444, 8-bit compression data, 8/10-bit raw RGB data
- **lens size:** 1/4"
- **lens chief ray angle:** 25° non-linear (see **table 10-1**)
- **input clock frequency:** 6 ~ 54 MHz
- **maximum image transfer rate:**
  QXGA (2048x1536): 15 fps for QXGA and any size scaling down from QXGA
  XGA (1024x768): 30 fps for XGA and any size scaling down from XGA
- **sensitivity:** 490 mV/(Lux • sec)
- **S/N ratio:** 36 dB
- **dynamic range:** 60 dB
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 1560 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 1.75 µm x 1.75 µm
- **well capacity:** 7.2 Ke^-
- **dark current:** <3 mV/sec @ 60°C
- **fixed pattern noise (FPN):** 1% of $V_{PEAK-TO-PEAK}$
- **image area:** 3626 µm x 2709 µm
- **package dimensions:** 6285 µm x 6125 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV3640 image sensor. The package information is shown in **section 9**.

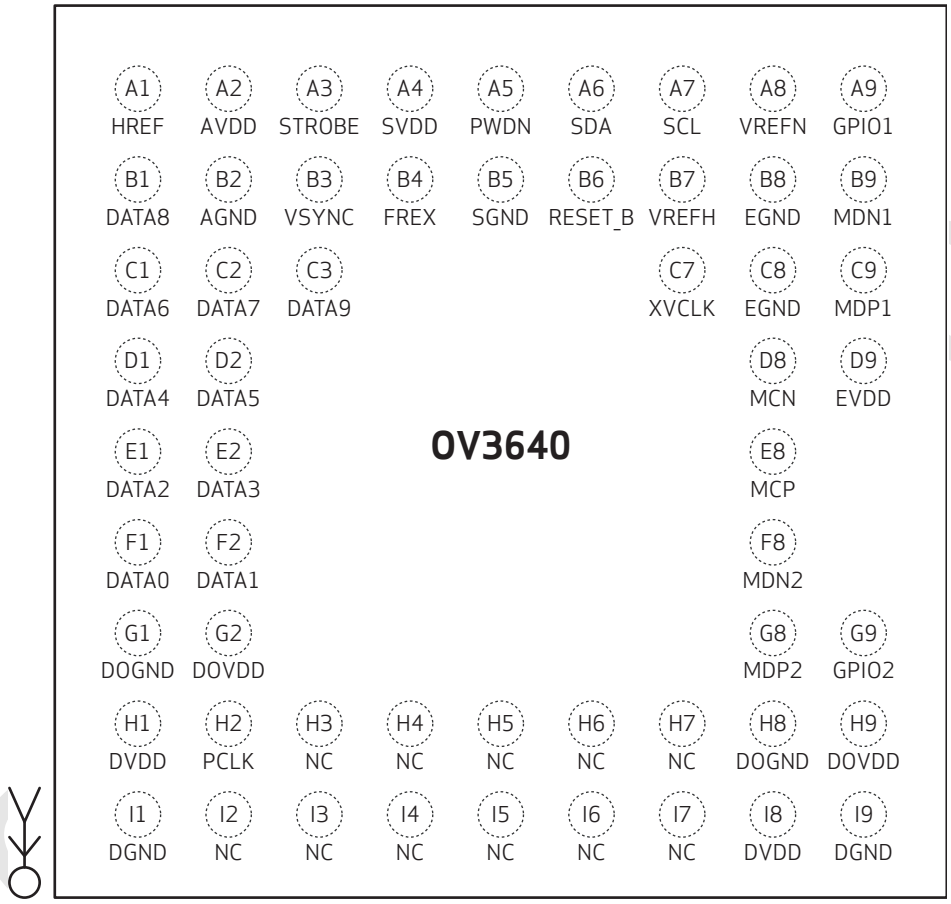
table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description	default I/O status
A1	HREF	I/O	horizontal reference output	input
A2	AVDD	power	analog power	
A3	STROBE	I/O	strobe output or scan chain test mode input	input
A4	SVDD	power	analog power	
A5	PWDN	input	power down active high with internal pull-down resistor	
A6	SDA	I/O	SCCB data	
A7	SCL	input	SCCB input clock	
A8	VREFN	reference	internal analog reference	
A9	GPIO1	I/O	general purpose I/O (GPIO) 1	input
B1	DATA8	I/O	digital video port (DVP) bit[8]	input
B2	AGND	ground	ground for analog circuit	
B3	VSYNC	I/O	vertical sync output	input
B4	FREX	I/O	anti-shake status output or OTP memory output	input
B5	SGND	ground	ground for sensor circuit	
B6	RESET_B	input	reset (active low with internal pull-up resistor)	
B7	VREFH	reference	internal analog reference	
B8	EGND	ground	ground for MIPI core	
B9	MDN1	output	MIPI first data lane negative output	
C1	DATA6	I/O	digital video port (DVP) bit[6]	input
C2	DATA7	I/O	digital video port (DVP) bit[7]	input
C3	DATA9	I/O	digital video port (DVP) bit[9]	input
C7	XVCLK	input	system input clock	
C8	EGND	ground	ground for MIPI core	
C9	MDP1	output	MIPI first data lane positive output	
D1	DATA4	I/O	digital video port (DVP) bit[4]	input
D2	DATA5	I/O	digital video port (DVP) bit[5]	input

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description	default I/O status
D8	MCN	output	MIPI clock lane negative output	
D9	EVDD	reference	power for MIPI core	
E1	DATA2	I/O	digital video port (DVP) bit[2]	input
E2	DATA3	I/O	digital video port (DVP) bit[3]	input
E8	MCP	output	MIPI clock lane positive output	
F1	DATA0	I/O	digital video port (DVP) bit[0]	input
F2	DATA1	I/O	digital video port (DVP) bit[1]	input
F8	MDN2	output	MIPI second data lane negative output	
G1	DOGND	ground	ground for I/O circuit	
G2	DOVDD	power	power for I/O circuit	
G8	MDP2	output	MIPI second data lane positive output	
G9	GPIO2	I/O	general purpose I/O (GPIO) 2	input
H1	DVDD	reference	power for digital core	
H2	PCLK	I/O	pixel clock output	input
H3	NC	–	no connect	
H4	NC	–	no connect	
H5	NC	–	no connect	
H6	NC	–	no connect	
H7	NC	–	no connect	
H8	DOGND	ground	ground for I/O circuit	
H9	DOVDD	power	power for I/O circuit	
I1	DGND	ground	ground for digital core	
I2	NC	–	no connect	
I3	NC	–	no connect	
I4	NC	–	no connect	
I5	NC	–	no connect	
I6	NC	–	no connect	
I7	NC	–	no connect	
I8	DVDD	reference	power for digital core	
I9	DGND	ground	ground for digital core	

figure 1-1 pin diagram



top view

2 system level description

2.1 overview

The OV3640 (color) image sensor is a low voltage, high-performance 1/4-inch 3.1 megapixel CMOS image sensor that provides the full functionality of a single chip QXGA (2048x1536) camera using OmniPixel3™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or arbitrarily scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface or MIPI interface.

The OV3640 has an image array capable of operating at up to 15 frames per second (fps) in QXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface, MIPI interface or embedded microcontroller. The OV3640 also includes a compression engine for increased processing power. In addition, Omnivision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

The OV3640 has an embedded microcontroller, which can be combined with an internal autofocus engine and programmable general purpose I/O modules (GPIO) for external autofocus control. It also provides an anti-shake function with an internal anti-shake engine. For storage purposes, the OV3640 also includes a one-time programmable (OTP) memory.

The OV3640 supports both a digital video parallel port and a serial MIPI port. The MIPI and ISP interface can be used for a second camera sensor without requiring a dual serial port camera system.

2.2 architecture

The OV3640 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV3640 image sensor. **figure 2-2** shows an example application using an OV3640 sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of the array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV3640 block diagram

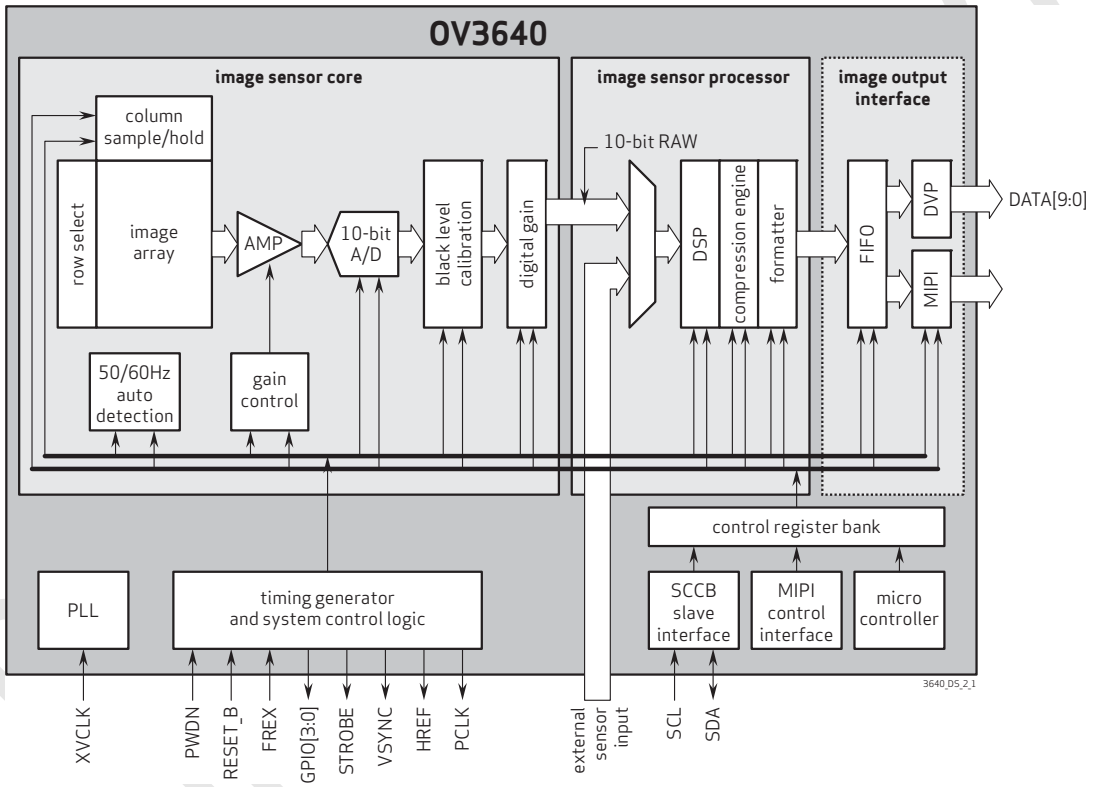
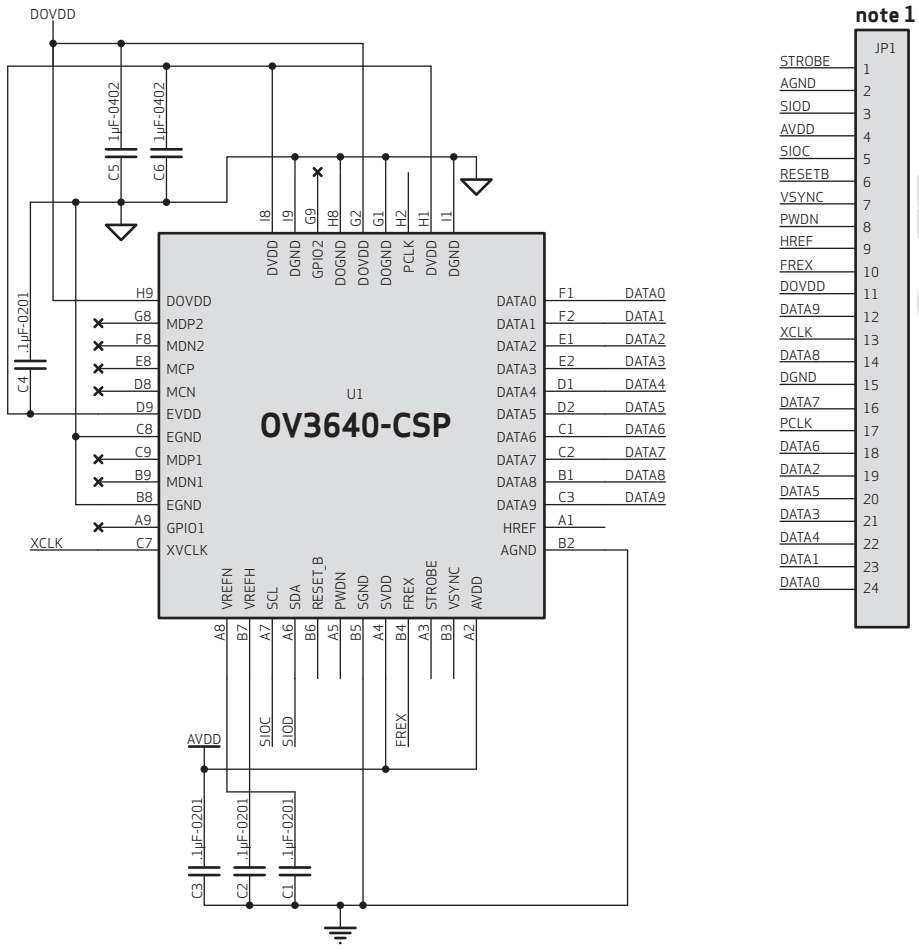


figure 2-2 reference design schematic



note 1 flex cable to molex 52437-2491

note 2 PWDN should be connected to ground outside of module if unused.
RESETB should be connected to DOVDD outside of module if unused.
Using internal DVDD is strongly recommended.
AVDD is 2.5 - 3.0V of sensor analog power (clean).
DOVDD is 1.81V +/- 5% of sensor digital IO power (clean).
AF_VCC is 3.3V of AF driver power.
sensor AGND and DGND should be separated and connected to a single point outside PCB (do not connect inside module).
capacitors should be close to related sensor pins.
DATA[9:0] is 10-bit sensor output (DATA9:MSB, DATA0:LSB).

note 3 if FREX pin is tied to ground, FREX pin should not be initialized as an output pin

3640_CSP_DS_2_2

2.3 I/O control

The OV3640 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pads.

table 2-1 driving capability and direction control for I/O pads

function	register	description
output drive capability control	0x30B2	Bit[1:0] output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
DATA[9:0] I/O control	0x30B1[1:0], 0x30B0[7:0]	input/output selection for the DATA[9:0] pins 0: input 1: output
GPIO2 I/O control	0x30B1	Bit[7] input/output selection for the GPIO2 pin 0: input 1: output
GPIO1 I/O control	0x30B1	Bit[6] input/output selection for the GPIO1 pin 0: input 1: output
VSYNC I/O control	0x30B1	Bit[5] input/output selection for the VSYNC pin 0: input 1: output
HREF I/O control	0x30B1	Bit[2] input/output selection for the HREF pin 0: input 1: output
PCLK I/O control	0x30B1	Bit[3] input/output selection for the PCLK pin 0: input 1: output
STROBE I/O control	0x30B1	Bit[4] input/output selection for the STROBE pin 0: input 1: output

2.4 power up sequence

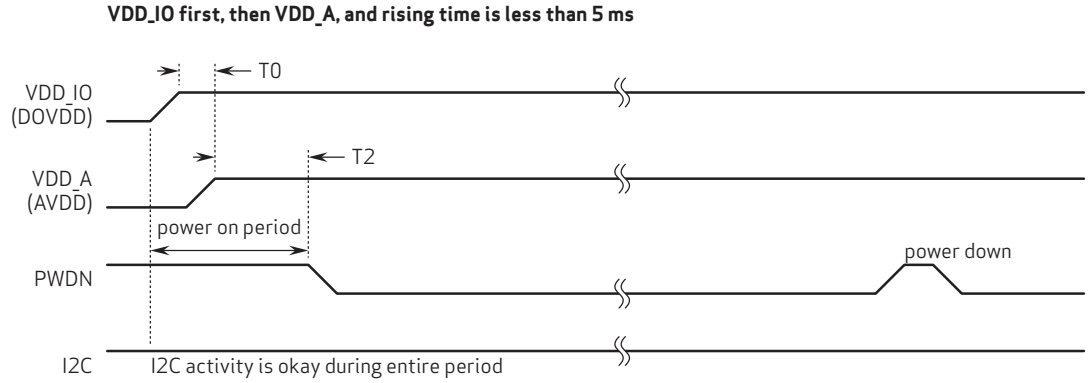
Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the I2C during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all powers, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.4.1 power up with internal DVDD and I2C access during power up period

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must go high if I2C is accessed during the power up period
4. for PWDN to go low, power up must first become stable (AVDD to PWDN ≥ 1 ms)
5. RESETB is active low with an asynchronized design
6. state of RESETB does not matter during power up period once DOVDD is up

figure 2-3 power up timing with internal DVDD and I2C access during power up period



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T2 ≥ 1 ms: delay from VDD_A stable to sensor power up stable

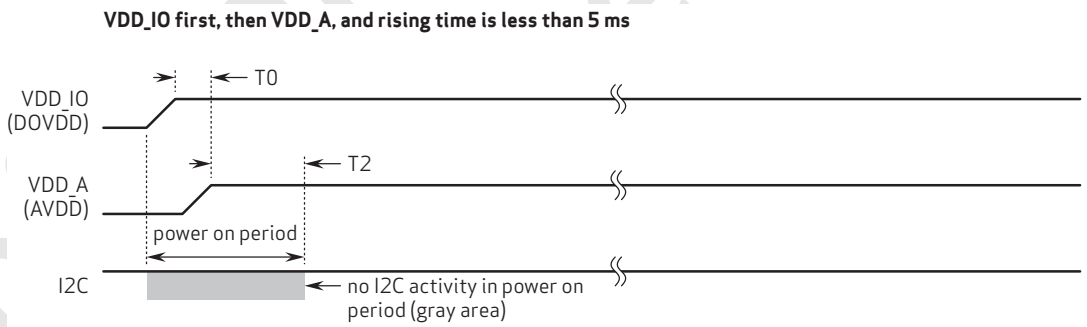
3640_DS_2_3

2.4.2 power up with internal DVDD and no I2C access during power up period

For powering up with the internal DVDD and no I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. PWDN is not required if there is no I2C access during the power up period
3. no I2C activity is allowed during the power up period (see gray area in **figure 2-4**)
4. RESETB is active low with an asynchronized design
5. state of RESETB does not matter during power up period once DOVDD is up

figure 2-4 power up timing with internal DVDD and no I2C access during power up period



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T2 ≥ 1 ms: delay from VDD_A stable to sensor power up stable

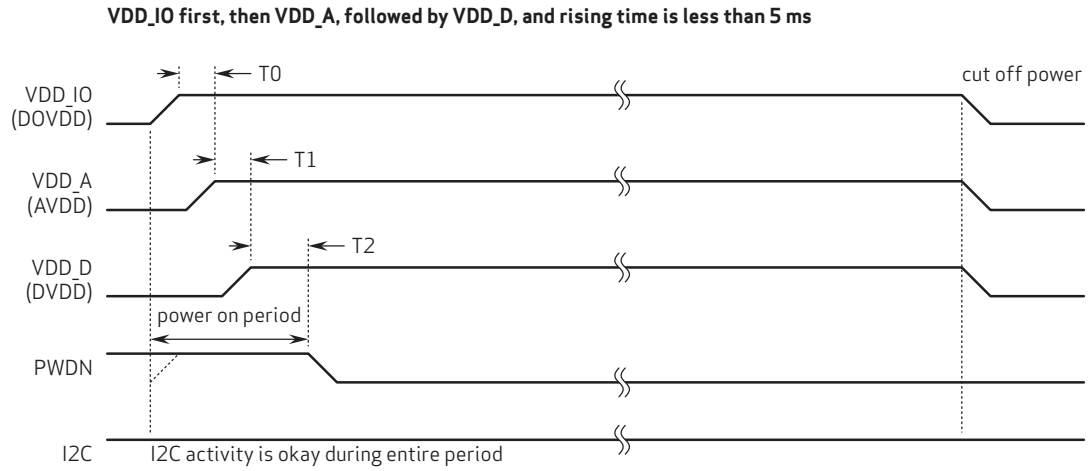
3640_DS_2_4

2.4.3 power up with external DVDD source and I2C access during power up period

For powering up with an external DVDD source and I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. if V_{DD-A} and V_{DD-D} are turned ON at the same time, make sure VDD-A becomes stable before V_{DD-D} becomes stable
3. PWDN is active high with an asynchronized design (does not need clock)
4. for PWDN to go low, power up must first become stable (DVDD to PWDN ≥ 1 ms)
5. all powers are cut off when the camera is not in use (power down mode is not recommended
6. RESETB is active low with an asynchronized design
7. state of RESETB does not matter during power up period once DOVDD is up

figure 2-5 power up timing with external DVDD source and I2C access during power up period



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T1 ≥ 0 ms: delay from VDD_A stable to VDD_C stable
T2 ≥ 1 ms: delay from VDD_C stable to sensor power up stable

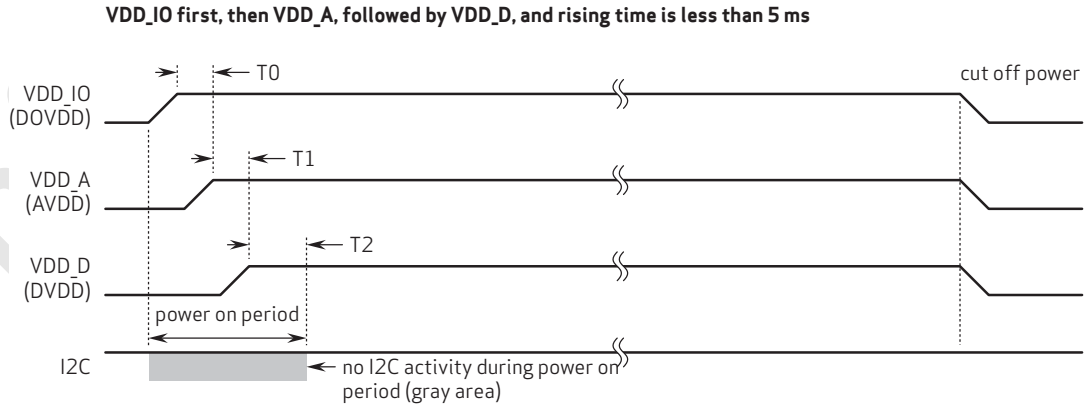
3640_DS_2_5

2.4.4 power up with external DVDD and no I2C access during power up period

For powering up with an external DVDD source and no I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. if V_{DD-A} and V_{DD-D} are turned ON at the same time, make sure VDD-A becomes stable before V_{DD-D} becomes stable
3. all powers are cut off when the camera is not in use (power down mode is not recommended
4. RESETB is active low with an asynchronized design
5. state of RESETB does not matter during power up period once DOVDD is up

figure 2-6 power up timing with external DVDD source and I2C access during power up period



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T1 ≥ 0 ms: delay from VDD_A stable to VDD_D stable
T2 ≥ 1 ms: delay from VDD_D stable to sensor power up stable

3640_DS_2_6

2.5 reset

The OV3640 sensor includes a **RESET_B** pin that forces a complete hardware reset when it is pulled low (GND). The OV3640 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x3012[7] to high.

The whole chip will be reset during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power up reset is included. The hard reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 1 ms.

2.6 standby and sleep

Two suspend modes are available for the OV3640:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the **PWDN** pin must be tied to high. When this occurs, the OV3640 internal device clock is halted and all internal counters are reset and registers are maintained. To avoid in-rush current on AVDD, power down the analog circuit by setting register 0x300E[7] to 1'b1 before pulling PWDN to high. For wakeup, after releasing PWDN pin from high to low, un-power down the analog circuit by setting register 0x300E[7] to 1'b0 to resume video. Refer to **section 2.6.1.1** below for the complete hardware standby procedure.

Executing a software power down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

The OV3640 also supports MIPI ultra low power state (ULPS). After receiving ULPS command from host, the OV3640 will enter into ULPS mode. Except for the low-speed part of the MIPI PHY and SCCB, all other blocks are enter into power down mode in ULPS mode.

2.6.1 1.8V I/O power

If I/O power is 1.8V, then using the internal DVDD is preferred. In this case, standby current is less than 40 µA.

2.6.1.1 hardware standby procedures

To enter standby mode:

78 300E B2 Enable bit[7]
78 308D 14
78 3086 0F
Pull PWDN pin to high to enter standby.

To return to normal mode:

Pull PWDN to low.
78 3086 08
78 308D 14
78 300E 32 Clear bit[7]

2.6.1.2 SCCB software sleep procedures

To enter standby mode:

78	300E	B2	Enable bit[7]
78	308D	14	
78	30AD	82	Enable bit[7]
78	3086	0F	

Stop input clock, MCLK, to enter sleep.

To return to normal mode:

Resume input clock, MCLK.

78	30AD	02	Clear bit[7]
78	3086	08	
78	308D	14	
78	300E	32	Clear bit[7]

2.6.2 2.6-2.8V I/O power

If I/O power is 2.6~2.8V, then an external DVDD source is preferred because of overheating issues related to the use of the internal DVDD. If an external 1.5V DVDD is provided, for single camera applications, cut off all powers when the sensor is not in use. For dual camera applications, when the second camera is in use, cutting off the OV3640 power may not be possible. Instead, power down the OV3640 and the power down current should be about 250 µA (for power down/sleep sequence, refer to **section 2.6.1.1** and **section 2.6.1.2**). When both cameras are not in use, cut off power to both cameras.

2.7 system clock control

The OV3640 PLL allows for an input clock frequency ranging from 6~54 MHz and has a maximum VCO frequency of 1.3 GHz. SysClk is the input clock for the sensor core, SerClk is for the MIPI and DvpClk is for the internal clock of the Image Signal Processing (ISP) block. The PLL can be bypassed by setting register 0x300F[3] to 1.

2.8 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

3 block level description

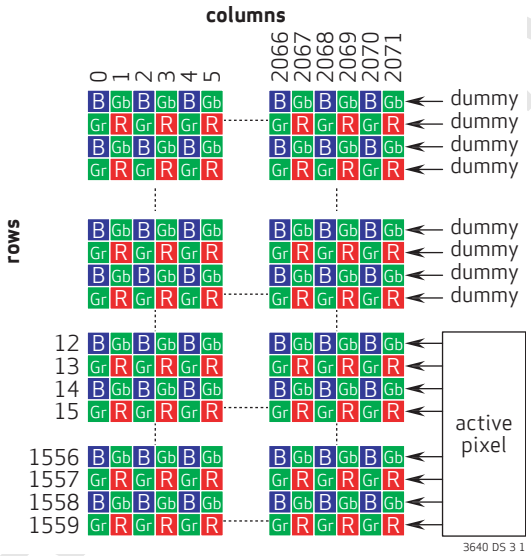
3.1 pixel array structure

The OV3640 sensor has an image array of 2072 columns by 1568 rows (3,248,896 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 3,248,896 pixels, 3,145,728 (2048x1536) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV3640 provides Mirror and Flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**). In mirror, since the Bayer order changes from BGBG... to GBGB..., the OV3640 usually delays the readout sequence by one pixel by setting register 0x397C[1] to 1. In flip, the OV3640 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make the necessary adjustments.

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

3640_DS_4_1

table 4-1 mirror and flip function control

function	register	description
mirror	0x307C	Bit[1] mirror ON/OFF select 0: mirror OFF 1: mirror ON
	0x3090	Bit[3] array mirror ON/OFF select 0: Array mirror OFF 1: Array mirror ON
flip	0x307C	Bit[0] flip ON/OFF select 0: flip OFF 1: flip ON
	0x3023	B/R row adjustment

4.2 image cropping

An image cropping area is defined by four parameters, HS (horizontal start), HW (horizontal width), VS (vertical start), VH (vertical height). By properly setting the parameters, any portion or size within the sensor array can be cropped as a visible area. This cropping is achieved by simply masking the pixels outside the cropping window; thus, it will not affect original timings. It will also not conflict with the flip and mirror functions.

figure 4-2 image cropping

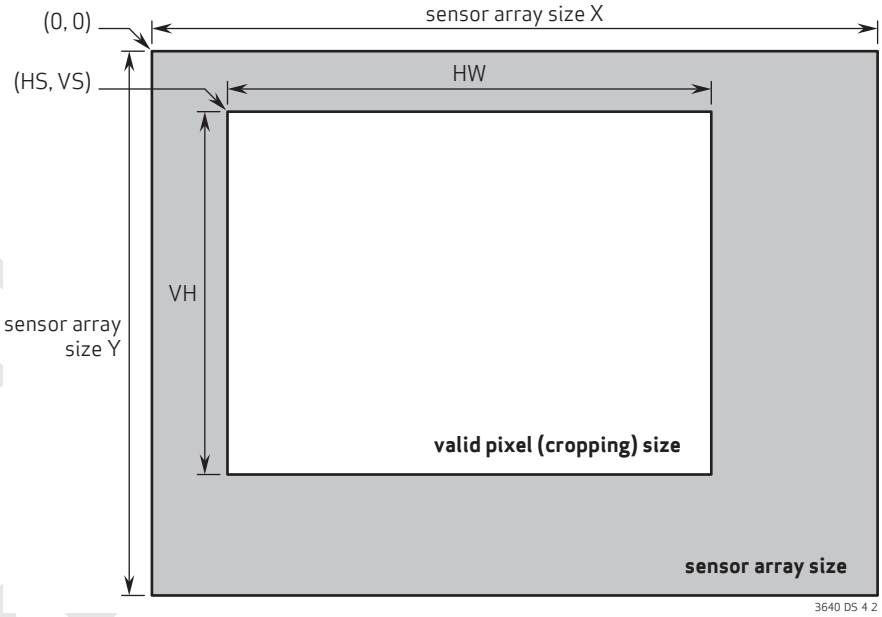


table 4-2 image cropping control functions

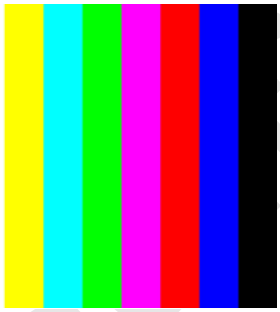
function	register	description
horizontal start	{0x3020, 0x3021}	HS[15:8] = 0x3020 HS[7:0] = 0x3021
vertical start[a]	{0x3022, 0x3023}	VS[15:8] = 0x3022 VS[7:0] = 0x3023
horizontal width	{0x3024, 0x3025}	HW[15:8] = 0x3024 HW[7:0] = 0x3025
vertical height	{0x3026, 0x3027}	VH[15:8] = 0x3026 VH[7:0] = 0x3027

a. VS can only be an even number

4.3 test pattern

For testing purposes, the OV3640 offers one type of test pattern, color bar.

figure 4-3 test pattern



color bar

table 4-3 test pattern selection control

function	register	description
test pattern ON/OFF	0x3080	Bit[7] test pattern ON/OFF select 0: OFF 1: ON
color bar	0x307B	Bit[1:0] color bar pattern select 10: color bar pattern
	0x307D	Bit[7] color bar enable 0: color bar OFF 1: color bar enable
	0x306C	Bit[4] color bar select 0: color bar 1: normal image

4.4 50/60hz detection

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50hz or 60hz light source so that the basic step of integration time can be determined.

4.5 AEC/AGC algorithms

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control.

4.6 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used to provide the data for black level calibration.

4.7 strobe flash control

To achieve the best image quality possible in low light conditions, the use of a strobe flash is recommended. The OV3640 provides a programmable strobe signal function.

4.7.1 sensor-controlled strobe flash

The OV3640 can generate a programmable strobe signal from the **STROBE** pin (pin **A3**). **table 4-4** lists the strobe pulse control registers.

table 4-4 strobe control functions

function	register	description
strobe function enable	**0x307A**	Bit[7]: strobe function enable 0: strobe disable 1: start strobe enable
strobe output pulse polarity control	**0x307A** (TMC4[6])	Bit[6]: strobe output polarity control 0: positive pulse 1: negative pulse
xenon mode strobe pulse width	**0x307A** (TMC4[3:2])	Bit[3:2]: xenon mode pulse width 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines
strobe mode	**0x307A** (TMC4[1:0])	Bit[1:0]: strobe mode select 00: xenon mode 01: LED 1 & 2 mode 10: LED 1 & 2 mode 11: LED 3 mode

4.7.1.1 strobe pulse

The strobe signal is programmable. It supports both LED and Xenon mode. The polarity of the pulse can be changed. The strobe signal is enabled (turned high / low depending on the pulse's polarity) by requesting the signal via the SCCB. Flash modules are typically triggered to the rising edge (falling edge, if signal polarity is changed). It supports the flashlight modes shown in **table 4-5**.

table 4-5 flashlight modes

function	register	description
xenon	one pulse	no
LED 1	pulse	no
LED 2	pulse	no
LED 3	continuous	yes

4.8 one time programmable (OTP) memory

The OV3640 supports a maximum of 128 bits of one-time programmable (OTP) memory to store chip identification and manufacturing information. Contact your local OmniVision FAE for more details.

5 image sensor processor digital functions

5.1 lens correction (LENC)

The main purpose of the LENC function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

5.2 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image. It supports manual white balance, simple AWB and advanced AWB. For advanced AWB settings, contact your local OmniVision FAE.

5.3 gamma curve (GMA)

The main purpose of the Gamma (GMA) function is to compensate for the non-linear characteristics of the sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions.

5.4 white black pixel cancellation (WBC)

The main purpose of White/Black pixel Cancellation (WBC) function is to remove the white/black pixels effect.

table 5-1 WBC-related registers

register address	register name	function
0x3301	DSP_CTRL_2	DSP Control 1 Bit[2]: WC_en This function removes the white pixels introduced by the sensor's defects. Bit[1]: BC_en This function removes the black pixels introduced by the sensor's defects.

5.5 interpolation/de-noise/edge enhancement (CIP)

The CIP functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. CIP functions work in both manual and auto modes.

5.6 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to convert images from the RGB domain to YUV domain. For different color temperatures, the parameters in the transmitting function will be changed.

5.7 zoom out (ZOOM)

The main purpose of the Zoom Out (ZOOM) function is to zoom out the image. According to the new_width and new_height of the new image, the module uses several pixels' values to generate one pixel's value. Some pixels' values are divided and used in two or more adjacent pixels. Calculating the algorithm uses finite float point to keep the mantissa when using this function.

5.8 special digital effects (SDE)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. Use SDE_CTRL to add some special effects to the image. Calculate the new U and V from Hue Cos, Hue Sin, and parameter signs. Saturate U and V using the Sat_u and Sat_v registers. Calculate Y using Yoffset, Ygain, and Ybright or set the Y value. SDE supports negative, black/white, sepia, greenish, blueish, reddish and other image effects which combine the effects already listed.

5.9 overlay

The OV3640 supports an overlay function.

5.10 autofocus (AFC)

AFC has three required functions:

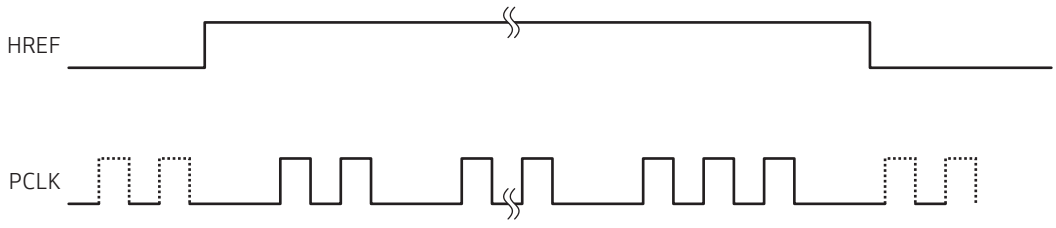
- local statistics - calculate maximum, minimum, and mean separately for R, G, and B in nine programmable zones
- histograms - calculates intensity histograms of R, G, and B pixels separately in at least three different programmable zones
- edge information - collects edge information for at least sixteen programmable zones

Contact your local OmniVision FAE for further details.

5.11 compression engine

5.11.1 compression mode 1 timing

figure 5-1 compression mode 1 timing



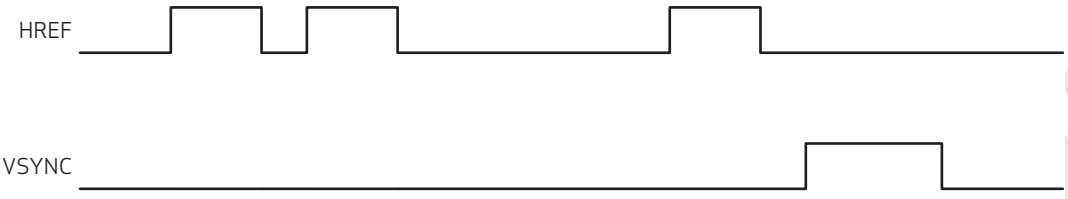
note 1 the whole frame has only one HREF
PCLK will be gated when there is no image data to transmit

3640_DS_5_5

5.11.2 compression mode 2 timing

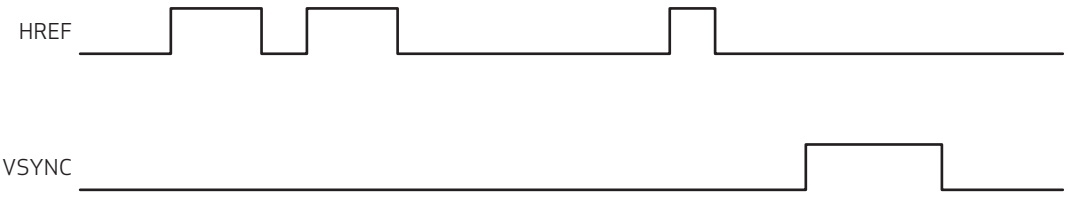
figure 5-2 compression mode 2 timing

a) dummy data padding at the last line



note 1 compression data is output with programmable width,
the last line may contain dummy data to match the width.
in each frame, the line numbers are different.

b) no dummy data padding at the last line



note 1 compression data is output with programmable width,
the last line may be less than others (there is no dummy data).
in each frame, the line numbers are different.

3640_DS_5_1

5.12 MCU description

Microprocessor firmware can be downloaded by writing to registers starting from 0x8000. A total of 6 KB of program memory can be used for program storage. Before downloading the firmware, the user must enable the MCU clock.

5.13 format description

Format control converts internal data format into the desirable output format including YUV, RGB, raw, compression data, HSYNC mode, etc.

table 5-2 format control register list (sheet 1 of 3)

register address	register name	function
0x3400	FMT_MUX_CTRL0	FMT_MUX_CTRL0 Bit[2:0]: Format input source select 000: DSP YUV444 001: DSP RGB888 010: DSP YUV422 011: DSP raw 100: Internal CIF raw 101: External CIF raw 110: External CIF YUV422 bypass 111: Not used
0x3403	ISP_PAD_CTRL2	ISP_PAD_CTRL2 Bit[7:4]: Xstart X start address for DVP windowing Bit[3:0]: Ystart Y start address for DVP windowing

table 5-2 format control register list (sheet 2 of 3)

register address	register name	function
0x3404	FMT_CTRL00	FMT_CTRL00 Bit[7]: UV_sel 0: Use UV_avg, Y 1: Use U0Y0, V0Y1 Bit[6]: YUV422_in Bit[5:0]: YUV422: 0x00: yuyvyuyv..../yuyvyuyv.... 0x01: yvyuyvyu..../yvyuyvyu.... 0x02: uyvyuyvy..../uyvyuyvy.... 0x03: vyuyvyuy..../vyuyvyuy.... YUV420: 0x04: yyyy..../yuyvyuyv.... 0x05: yyyy..../yvyuyvyu.... 0x06: yyyy..../uyvyuyvy.... 0x07: yyyy..../vyuyvyuy.... 0x08: yuyvyuyv..../yyyy.... 0x09: yvyuyvyu..../yyyy.... 0x0A: uyvyuyvy..../yyyy.... 0x0B: vyuyvyuy..../yyyy.... 0x0C: uyyuyy..../vyyvyy Y8: 0x0D: yyyy..../yyyy.... YUV444 (RGB888) 0x0E: yuvyuv..../yuvyuv.... (gbrgbr..../gbrgbr....) 0x0F: yvuyvu..../yvuyvu.... (grbgrb..../grbgrb....) 0x1C: uyvuyv..../uyvuyv.... (bgrbgr..../bgrbgr....) 0x1D: vyuvyu..../vyuvyu.... (rgbrgb..../rgbrgb....) 0x1E: uvyuvy..../uvyuvy.... (brgbrg..../brgbrg....) 0x1F: vuyvuy..../vuyvuy.... (rbgrbg..../rbgrbg....) RGB565: 0x10: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x11: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x30: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} (MIPI RGB565) RGB555: 0x12: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x13: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]} 0x32: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} RGB444: 0x14: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x15: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x34: {g[0],2'h0,b[3:0],1'b0}, {r[3:0],1'b0,g[3:1]} (MIPI RGB444) 0x37: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x38: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x16: {b[3:0],g[3:0]}, {r[3:0],b[3:0]} ... 0x17: {r[3:0],g[3:0]}, {b[3:0],r[3:0]} ... RAW: 0x18: bgbg..../grgr.... 0x19: gbgb..../rgrg.... 0x1A: grgr..../bgbg.... 0x1B: rgrg..../gbgb....

table 5-2 format control register list (sheet 3 of 3)

register address	register name	function
0x3405	DITHER_CTRL0	DITHER_CTRL0 Bit[6]: Dither_sel 0: Use register setting 1: Dithering according to fmt_control Bit[5:4]: R_dithering 00: No dithering 01: 4-bit 10: 5-bit 11: 6-bit Bit[3:2]: G_dithering 00: No dithering 01: 4-bit 10: 5-bit 11: 6-bit Bit[1:0]: B_dithering 00: No dithering 01: 4-bit 10: 5-bit 11: 6-bit

6 image sensor output interface digital functions

6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported and extended features including compression mode, HSYNC mode and test pattern output.

6.1.2 DVP timing

figure 6-1 DVP timing diagram

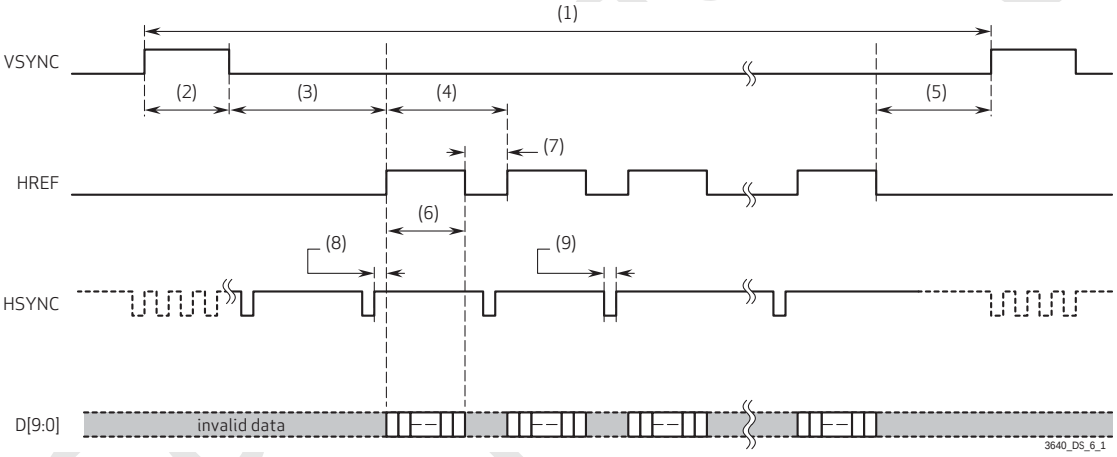


table 6-1 DVP timing specifications (sheet 1 of 2)

mode	timing
QXGA 2048x1536	(1) 3725568 tp ≅ 1568 tline (2) 2048 tp (4 tline = 2376 × 4 = 9504 tp in HSYNC mode) (3) 28724 tp (4) 2376 tp (5) 45588 tp (6) 2048 tp (7) 328 tp (8) 0 tp (9) 328 tp where tp = t_{PCLK}

note
The timing values shown in **table 6-1** may vary depending upon register settings.

table 6-1 DVP timing specifications (sheet 2 of 2)

mode	timing
UXGA 1600x1200	(1) 2901177 tp ≅ 1221 tline (2) 2048 tp (3) 31638 tp (4) 2376 tp (5) 17067 tp (6) 1600 tp (7) 776 tp (8) 0 tp (9) 776 tp where tp = t_{PCLK}
XGA 1024x768 (PCLK/2)	(1) 1849715 tp ≅ 779 tline (2) 2048 tp (4 tline = 2376 x 4 = 9504 tp in HSYNC mode) (3) 15787 tp (4) 2376 tp (5) 8464 tp (6) 1024 tp (7) 1352 tp (8) 0 tp (9) 1352 tp where tp = t_{PCLK} × 2
SQCIF 128x96 (PCLK/14)	(1) 264300 tp ≅ 97 tline (2) 2048 tp (3) 2967 tp (4) 2716 tp (5) 1137 tp (6) 128 tp (7) 2588 tp (8) 0 tp (9) 2588 tp where tp = t_{PCLK} × 4

6.1.3 DVP image formats

6.1.3.1 YUV422 format

Uncompressed YUV422 data is sent out through DATA[9:2] and the sequence can be YUYV, UYVY, YVYU, VYUY.

table 6-2 YUYV format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]
odd	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]

table 6-3 UYVY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]
odd	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]

table 6-4 YVYU format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]
odd	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]

table 6-5 VYUY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]
odd	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]

6.1.3.2 YUV420 format

The data format of uncompressed YUV420 is similar to that of uncompressed YUV422 except that UV data of either even or odd lines is dropped by de-asserting PCLK.

6.1.3.3 Y8 format

Uncompressed Y8 data is sent out through DATA[9:2]. The frequency of PCLK is the same as that of raw data or half of YUV422/420.

6.1.3.4 RGB565 format

Uncompressed RGB565 data is sent out through DATA[9:2].

table 6-6 RGB565 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	G2	B7	B6	B5	B4	B3

6.1.3.5 RGB555 format

table 6-7 RGB555 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	0	B7	B6	B5	B4	B3

6.1.3.6 RGB444 format

The data format of uncompressed RGB444 is similar to RGB565 except that the lowest bit of R, B, and the lowest 2 bits of G are dummy bits.

table 6-8 RGB444 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	X	X	X	X	R7	R6	R5	R4
odd	G7	G6	G5	G4	B7	B6	B5	B4

6.2 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. Two data lanes have full support for HS (uni-directional) and LP (bi-directional) data transfer mode. Contact your local OmniVision FAE for more details.

7 register tables

The following tables provide descriptions of the device control registers contained in the OV3640. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x78 for write and 0x79 for read.

table 7-1 system control registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x3000	AGC[15:8]	0x00	RW	Auto Gain Control Bit[7:0]: AGC RSVD gain register
0x3001	AGC[7:0]	0x00	RW	Auto Gain Control - AGC[7:0] Bit[7:0]: Actual Gain – Range from 1x to 32x Gain = (Bit[7]+1) × (Bit[6]+1) × (Bit[5]+1) × (Bit[4]+1) × (1+Bit[3:0]/16) Set Auto1[2] (R**0x3013**[2]) = 0 to disable AGC.
0x3002	AEC[15:8]	0x00	RW	Auto Exposure Control - AEC[15:8]
0x3003	AEC[7:0]	0x01	RW	Auto Exposure Control - AEC[7:0] AEC[15:0]: Exposure time Tex = Tline × AEC[15:0] Tline ≤ Tex ≤ 1 frame period The maximum exposure time will be 1 frame period even if Tex is set longer than 1 frame period. Set Auto1[0] (R**0x3013**[0]) = 0 to disable AEC.
0x3004	AECL[7:0]	0x00	RW	Manual Extreme Bright Exposure Control - AECL[7:0] In extremely bright conditions where Tex must be less than Tline, the exposure time may be set manually by this control. Tex = Tline – L1AEC[7:0] steps Tex min. ≤ Tex ≤ Tline Set Auto2[1] (R**0x3014**[1]) = 1 to enable manual AECL.
0x3005~ 0x3009	RSVD	–	–	Reserved
0x300A	PIDH	0x36	RW	Product ID MSBs (read only)
0x300B	PIDL	0x4C	RW	Product ID LSBs (read only) for REV2c. For REV2a, this register should be 0x41. For REV1a, this register should be 0x40.
0x300C	SCCB ID	0x78	RW	SCCB ID

table 7-1 system control registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x3011	CLK[7:0]	0x00	RW	Clock Rate Control Bit[7]: Digital frequency doubler 0: OFF 1: ON Bit[6]: PLL and clock divider bypass 0: Master mode, sensor provides PCLK 1: Slave mode, external PCLK input from XVCLK pin Bit[5:0]: Clock divider CLK = XVCLK/(decimal value of CLK[5:0] + 1)
0x3012	SYS[7:0]	0x00	RW	Format Control Bit[7]: SRST 1: Initiates soft reset. All registers are set to factory default values after which the chip resumes normal operation. Bit[6:4]: Sensor array resolution 000: QXGA (full size) mode 001: XGA mode Bit[3]: Reserved Bit[2:0]: Output format selection (not used)

table 7-1 system control registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x3013	AUTO_1[7:0]	0xE7	RW	Auto Control 1 Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: AEC speed/step selection 0: Small steps, slow 1: Big steps, fast Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure to 1/120s Bit[4]: Auto banding filter 0: Banding filter is always ON/OFF depending on AUTO_1[5] (R0x3013[5]) setting 1: Automatically disable the banding filter under strong light condition Bit[3]: Extreme bright exposure control enable 0: OFF, Tline <= Tex min. 1: ON, enable minimum exposure Tex min. ≤ Tline Bit[2]: Auto gain control auto/manual mode selection 0: Manual 1: Auto Bit[1]: Not used Bit[0]: Auto exposure control auto/manual mode selection 0: Manual 1: Auto

table 7-1 system control registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x3014	AUTO_2[7:0]	0x04	RW	Auto Control 2 Bit[7]: Manually assign banding 0: 60Hz 1: 50Hz Bit[6]: Auto banding detection enable 0: Banding according to AUTO_2[7] (**0x3014**[7]) manual setting 1: Banding depending on auto 50/60 Hz detection result Bit[5]: Reserved Bit[4]: Freeze AEC/AGC Bit[3]: Night mode enable 0: Disable 1: Enable Bit[2]: BDcAEC - enable banding AEC smooth switch between 50/60 Bit[1]: Manually assign extreme bright exposure enable 0: Auto exposure 1: Exposure based on AECL[7:0] (**0x3014**[7:0]) steps Bit[0]: Banding filter option 0: Disable 1: Enable
0x3015	AUTO_3[7:0]	0x02	RW	Auto Control 3 Bit[7]: Not used Bit[6:4]: Dummy frame control 000: No dummy frame 001: Allow 1 dummy frame 010: Allow 2 dummy frames 011: Allow 3 dummy frames 100: Allow 7 dummy frames Bit[3]: Not used Bit[2:0]: AGC gain ceiling, GH[2:0] 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x 111: 128x

table 7-1 system control registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x3018	WPT/HISH[7:0]	0x78	RW	Luminance Signal/Histogram High Range for AEC/AGC operation Shared by average and histogram based algorithm AEC/AGC value decreases in auto mode when average luminance/histogram is greater than WPT/HisH[7:0]
0x3019	BPT/HISL[7:0]	0x68	RW	Luminance Signal/Histogram Low Range for AEC/AGC operation Shared by average and histogram based algorithm AEC/AGC value increases in auto mode when average luminance/histogram is less than BPT/HisL[7:0]
0x301A	VPT[7:0]	0xD4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VPT[7:4] or less than VPT[3:0]
0x301B	YAVG	0x00	RW	Luminance Average - this register will auto update Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) × 0.25
0x301C	AECG_MAX50	0x05	RW	50 Hz Smooth Banding Maximum Steps Control Bit[7:6]: Reserved Bit[5:0]: AECG_MAX50[5:0] 50 Hz smooth banding maximum steps
0x301D	AECG_MAX60	0x07	RW	60 Hz Smooth Banding Maximum Steps Control Bit[7:6]: Reserved Bit[5:0]: AECG_MAX60[5:0] 60 Hz smooth banding maximum steps
0x3020	HS[15:8]	0x01	RW	Horizontal Window Start 8 MSBs HS[15:0]: Horizontal start point of array, each bit represents 1 pixel

table 7-1 system control registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x3021	HS[7:0]	0x1D	RW	Horizontal Window Start 8 LSBs HS[15:0]: Horizontal start point of array, each bit represents 1 pixel
0x3022	VS[15:8]	0x00	RW	Vertical Window Start 8 MSBs VS[15:0]: Vertical start point of array, each bit represents 1 scan line **Note:** VS[15:0] can only be an even number.
0x3023	VS[7:0]	0x0A	RW	Vertical Window Start 8 LSBs VS[15:0]: Vertical start point of array, each bit represents 1 scan line **Note:** VS[15:0] can only be an even number.
0x3024	HW[15:8]	0x18	RW	Horizontal Width 8 MSBs HW[15:0]:Output raw image pixels are from HS[15:0] to HS[15:0] + HW[15:0]
0x3025	HW[7:0]	0x00	RW	Horizontal Width 8 LSBs HW[15:0]:Output raw image pixels are from HS[15:0] to HS[15:0] + HW[15:0]
0x3026	VH[15:8]	0x06	RW	Vertical Height 8 MSBs VH[15:0]: Output raw image pixels are from VS[15:0] to VS[15:0] + VH[15:0]
0x3027	VH[7:0]	0x0C	RW	Vertical Height 8 LSBs VH[15:0]: Output raw image pixels are from VS[15:0] to VS[15:0] + VH[15:0]
0x3028	HTS[15:8]	0x09	RW	Horizontal Total Size 8 MSBs HTS[15:0]:Horizontal total size for 1 line
0x3029	HTS[7:0]	0x47	RW	Horizontal Total Size 8 LSBs HTS[15:0]:Horizontal total size for 1 line
0x302A	VTS[15:8]	0x06	RW	Vertical Total Size 8 MSBs VTS[15:0]:Vertical total size for 1 frame
0x302B	VTS[7:0]	0x20	RW	Vertical Total Size 9 LSBs VTS[15:0]:Vertical total size for 1 frame
0x302D	EXVTS[15:8]	0x00	RW	VSYNC Pulse Width 8 MSBs EXVTS[15:0]:Line periods added to VSYNC width. Default VSYNC output width is 4 × tline. Each LSB count will add 1 × Tline to the VSYNC active period.

table 7-1 system control registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x302E	EXVTS[7:0]	0x00	RW	VSYNC Pulse Width LSB 8 bits EXVTS[15:0]:Line periods added to VSYNC width. Default VSYNC output width is 4 × tline. Each LSB count will add 1 × Tline to the VSYNC active period.
0x3070	BD50[15:8]	0x00	RW	50Hz Banding 8 MSBs 50Hz = 1 / (BD50[15:0] × Tline)
0x3071	BD50[7:0]	0xEB	RW	50Hz Banding 8 LSBs 50Hz = 1 / (BD50[15:0] × Tline)
0x3072	BD60[15:8]	0x00	RW	60Hz Banding 8 MSBs 60Hz = 1 / (BD60[15:0] × Tline)
0x3073	BD60[7:0]	0xC4	RW	60Hz Banding 8 LSBs 60Hz = 1 / (BD60[15:0] × Tline)
0x3077	TMC1	0x00	RW	Timing Control 1 Bit[7]: CHSYNC pin output swap 0: CHSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: CHSYNC Bit[5:4]: Reserved Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
0x307A	TMC4	0x00	RW	Timing Control 4 Bit[7:0]: RSTRB[7:0] Flash light control
0x307B	TMC5	0x40	RW	Timing Control 5 Bit[7:4]: Reserved Bit[3]: Digital color bar enable Bit[2:0]: Pattern Select digital color bar pattern

table 7-1 system control registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x307C	TMC6	0x10	RW	Timing Control 6 Bit[7:2]: Reserved Bit[1]: Horizontal mirror Bit[0]: Vertical flip
0x307D	TMC7	0x20	RW	Timing Control 7 Bit[7]: Color bar test pattern 0: OFF 1: ON Bit[6:0]: Reserved
0x3080	TMCA	0x11	RW	Timing Control A Bit[7]: Output pattern option Bit[6:0]: Reserved
0x3081	TMCB	0x04	RW	Timing Control B Bit[7]: MIRROR_OPT Pixel shift while mirroring 0: OFF 1: ON Bit[6]: OTP memory clock option 0: Slow 1: Fast Bit[5:1]: Reserved Bit[0]: Swap MSB and LSB at the output port
0x3086	TMC10	0x00	RW	Timing Control 10 Bit[7:4]: Reserved Bit[3]: Wakeup reset enable Bit[2]: RegSleep option Bit[1]: Sleep option Bit[0]: Sleep ON/OFF 0: OFF 1: ON
0x3088	ISP_XOUT[15:8]	0x80	RW	ISP X-direction Output Size [15:8] Bit[7:4]: Not used Bit[3:0]: X_size_in[11:8]
0x3089	ISP_XOUT[7:0]	0x00	RW	ISP X-direction Output Size [7:0]
0x308A	ISP_YOUT[15:8]	0x06	RW	ISP Y-direction Output Size [15:8] Bit[7:3]: Not used Bit[2:0]: X_size_in[10:8]
0x308B	ISP_YOUT[7:0]	0x00	RW	ISP Y-direction Output Size [7:0]
0x308C	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x308D	TMC13	0x00	RW	Timing Control 13 Bit[7]: RegSleep setting Bit[6:2]: Reserved Bit[1]: RegSleep option Bit[0]: Reserved
0x308F	OTP	–	R	OTP Memory Internal Registers Data Readout
0x3090~ 0x30A8	RSVD	–	–	Reserved
0x30A9	PWCOM1	0xB5	RW	Power Common Control 1 Bit[7:4]: Reserved Bit[3]: Bypass regulator Bit[2:0]: Reserved
0x30AA~ 0x30AF	RSVD	–	–	Reserved
0x30B0	IO_CTRL0	0x00	RW	IO Control 0 Bit[7:0]: CY[7:0]
0x30B1	IO_CTRL1	0x00	RW	IO Control 1 Bit[7:6]: C_GP[1:0] Bit[5]: C_VSYNC Bit[4]: C_STROBE Bit[3]: C_PCLK Bit[2]: C_HREF Bit[1:0]: CY[9:8]
0x30B2	IO_CTRL2	0x00	RW	IO Control 2 GPO_monitor, C_FREX, R_PAD[3:0]
0x30B3	RSVD	–	–	Reserved
0x30B4	DVP0	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: GPO[3:0]

table 7-2 FMT_MUX registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3400	FMT_MUX_CTRL0	0x03	RW	Bit[7:3]: Reserved Bit[2:0]: Fmt_sel 000: ISP YUV 001: ISP RGB 010: ISP YUV422 011: ISP RAW 100: Int CIF RAW 101: Ext CIF RAW 110: Ext CIF YUV422 bypass
0x3401~ 0x3402	RSVD	–	–	Reserved
0x3403	ISP_PAD_CTR2	0x42	RW	Bit[7:4]: X start Bit[3:0]: Y start
0x3404	FMT_CTRL00	0x18	RW	Bit[7] UV_sel 0: Use UV_avg, Y 1: Use U0Y0, V0Y1 Bit[6]: YUV422_in 0: Input to FORMAT is raw data 1: Input to FORMAT is YUV422 data when bypassing FORMAT Bit[5:0]: YUV422: 0x00: yuyvyuyv..../yuyvyuyv.... 0x01: yvyuyvyu..../yvyuyvyu.... 0x02: uyvyuyvy..../uyvyuyvy.... 0x03: vyuyvyuy..../vyuyvyuy.... YUV420: 0x04: yyyy..../yuyvyuyv.... 0x05: yyyy..../yvyuyvyu.... 0x06: yyyy..../uyvyuyvy.... 0x07: yyyy..../vyuyvyuy.... 0x08: yuyvyuyv..../yyyy.... 0x09: yvyuyvyu..../yyyy.... 0x0A: uyvyuyvy..../yyyy.... 0x0B: vyuyvyuy..../yyyy.... 0x0C: uyyuyy..../vyyvyy Y8: 0x0D: yyyy..../yyyy....

table 7-2 FMT_MUX registers (sheet 2 of 3)

address	register name	default value	R/W	description
				YUV444(RGB888): 0x0E: yuvyuv..../yuvyuv.... (gbrgbr..../gbrgbr....) 0x0F: yvuyvu..../yvuyvu.... (grbgrb..../grbgrb....) 0x1C: uyvuyv..../uyvuyv.... (bgrbgr..../bgrbgr....) 0x1D: vyuvyu..../vyuvyu.... (rgbrgb..../rgbrgb....) 0x1E: uvyuvy..../uvyuvy.... (brgbrg..../brgbrg....) 0x1F: vuyvuy..../vuyvuy.... (rbgrbg..../rbgrbg....) RGB565: 0x10: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x11: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x30: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} (MIPI RGB565) RGB555: 0x12: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x13: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0] 0x32: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} (MIPI RGB555) RGB444: 0x14: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x15: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x34: {g[0],2'h0,b[3:0],1'b0}, {r[3:0],1'b0,g[3:1]} (MIPI RGB444) 0x37: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x38: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x16: {b[3:0],g[3:0]}, {r[3:0],b[3:0]} ... 0x17: {r[3:0],g[3:0]}, {b[3:0],r[3:0]} ... Raw: 0x18: bgbg..../grgr.... 0x19: gbgb..../rgrg.... 0x1A: grgr..../bgbg.... 0x1B: rgrg..../gbgb....

table 7-2 FMT_MUX registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3405	DITHER_CTRL0	0x40	RW	Bit[7]: Reserved Bit[6]: Dither_sel 0: Use register seting 1: Follow with fmt_control Bit[5:4]: R_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit Bit[3:2]: G_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit Bit[1:0]: B_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit

8 electrical specifications

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
operating temperature range[b]		-20°C to +70°C
stable operating temperature range[c]		0°C to +50°C
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

b. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

c. image quality remains stable throughout this temperature range

table 8-2 DC characteristics (-20°C < T_A < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.5	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}[b]	supply voltage (digital I/O)	1.7	1.8	3.0	V
I_{DD-A}	active (operating) current		35	50[c]	mA
I_{DD-IO}[d, e]			95	125[f]	mA
P_O	active (operating) power consumption			360[g]	mW
$I_{DDS-SCCB}$[h]	standby current		20	40	µA
$I_{DDS-PWDN}$[h]			20	40	µA
$P_{DDS-SCCB}$	standby power consumption			112	µW
$P_{DDS-PWDN}$				112	µW
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs[i]					
V_{IL}	SCL and SDA	-0.5	0	0.54	V
V_{IH}	SCL and SDA	1.26	1.8	3.0	V

a. using the internal DVDD regulator is strongly recommended for minimum power down current

b. using 1.8V for V_{DD-IO} is strongly recommended; to use 2.8V for V_{DD-IO}, contact your local OmniVision FAE for details

c. maximum in-rush current on AVDD is 100 mA

d. active current is based on sensor resolution at full size and at full speed in compression format

e. with MIPI function, the active current needs an additional 20mA

f. maximum in-rush current on DOVDD is 200 mA

g. active power consumption value is based on 1.8V V_{DD-IO}

h. at room temperature and typical supply voltages

i. based on DOVDD = 1.8V.

table 8-3 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)[a]	6	24	54	MHz
t_r, t_f	clock input rise/fall time			5 (10[b])	ns

a. for input clock range 6~27MHz, OV3640 can tolerate input clock jitter up to 1ns

b. if using the internal PLL

figure 8-1 SCCB interface timing

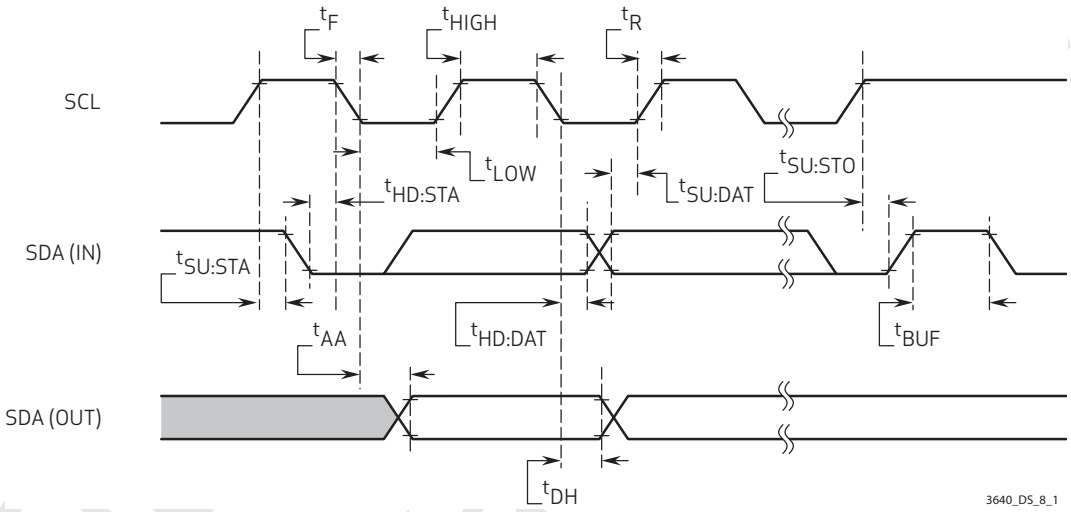


table 8-5 SCCB interface timing specifications[a]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400[b]	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	1.85			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. SCCB maximum speed is 400KHz when sensor master input clock (XVCLK) is greater than or equal to 13MHz. When XVCLK is less than 13MHz, the maximum SCCB speed is less than 400KHz (approximately XVCLK/32.5)

figure 8-2 line/pixel output timing

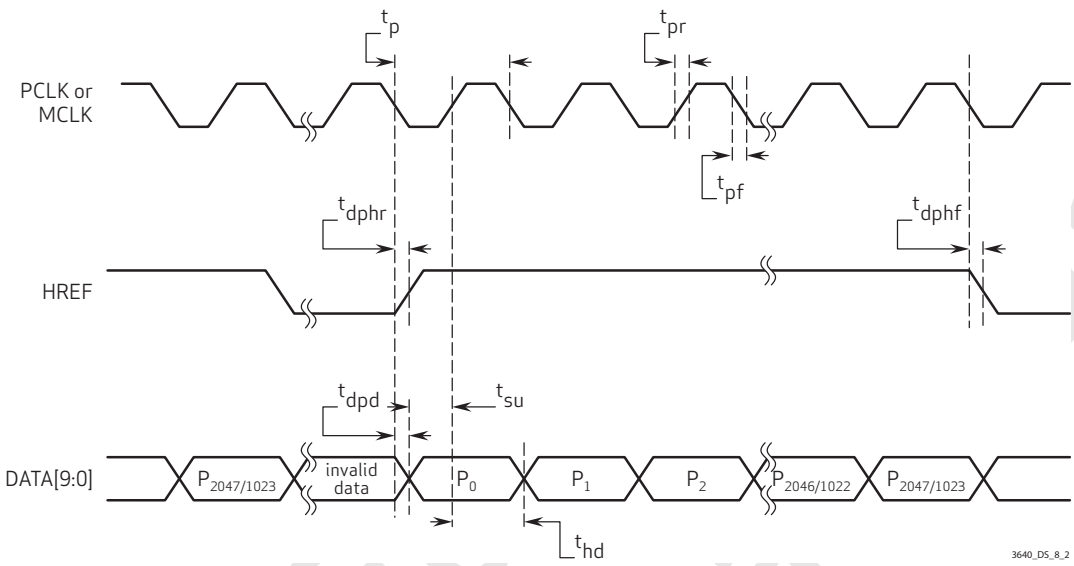


table 8-6 pixel timing specifications

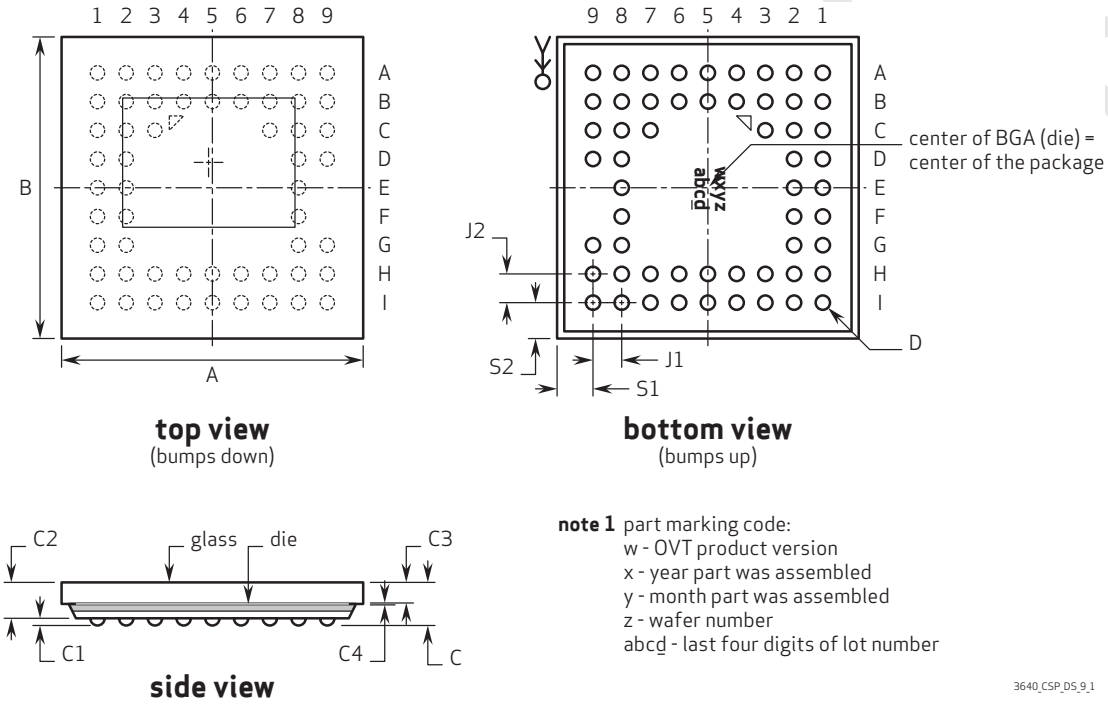
symbol	parameter	min	typ	max	unit
t_p	PCLK period[a]		17.86		ns
t_{pr}	PCLK rising time[a]		2		ns
t_{pf}	PCLK falling time[a]		2		ns
t_{dphr}	PCLK negative edge to HREF rising edge		4		ns
t_{dphf}	PCLK negative edge to HREF negative edge		2		ns
t_{dpd}	PCLK negative edge to data output delay	1		4	ns
t_{su}	data bus setup time	4	6		ns
t_{hd}	data bus hold time	10	12		ns

a. PCLK running at 56MHz, C_L = 15pF, and DOVDD = 1.8V

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications



note 1 part marking code:
w - OVT product version
x - year part was assembled
y - month part was assembled
z - wafer number
abcd - last four digits of lot number

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table 9-1 package dimensions (sheet 1 of 2)

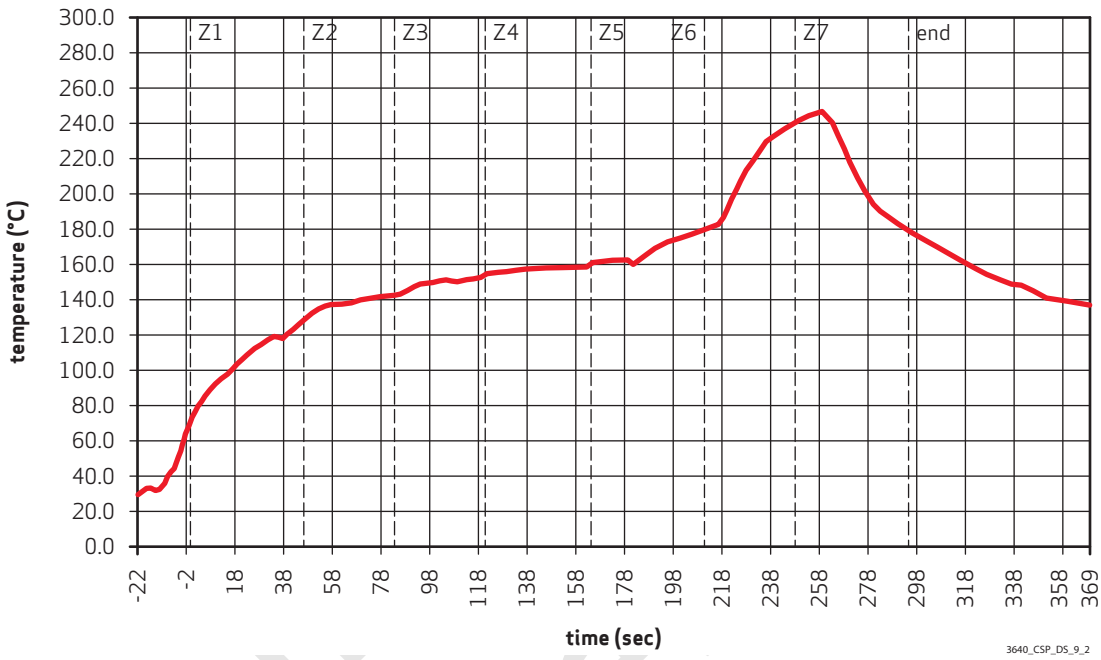
parameter	symbol	min	typ	max	unit
package body dimension x	A	6260	6285	6310	µm
package body dimension y	B	6100	6125	6150	µm
package height	C	825	885	945	µm
ball height	C1	130	160	190	µm
package body thickness	C2	680	725	770	µm
cover glass thickness	C3	375	400	425	µm
airgap between cover glass and sensor	C4	30	45	60	µm
ball diameter	D	270	300	330	µm

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
total pin count	N		56 (11 NC)		
pin count x-axis	N1		9		
pin count y-axis	N2		9		
pins pitch x-axis	J1		610		µm
pins pitch y-axis	J2		610		µm
edge-to-pin center distance analog x	S1	673	703	733	µm
edge-to-pin center distance analog y	S2	593	623	653	µm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note
The OV3640 uses a lead-free package.

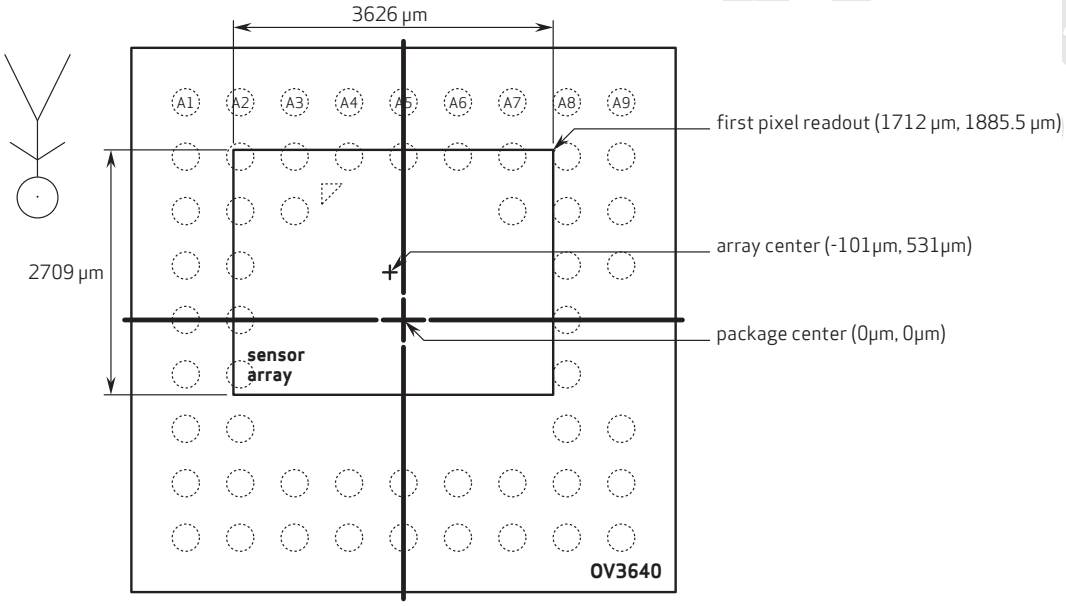
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A9 oriented down on the PCB.

3640_CSP_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

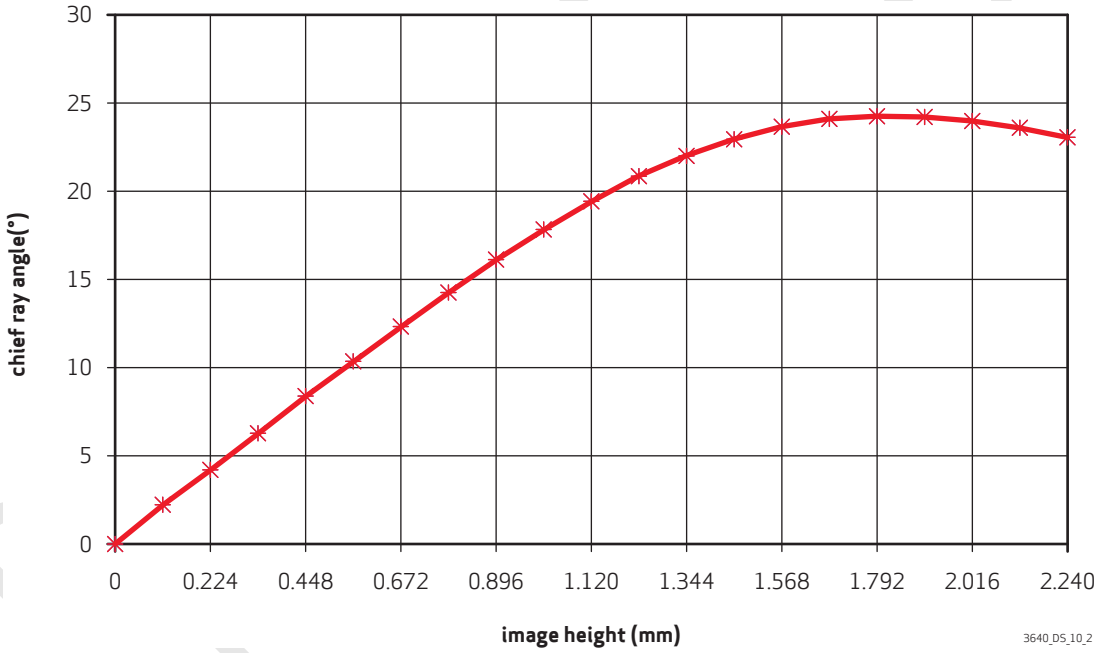


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.05	0.112	2.18
0.1	0.224	4.2
0.15	0.336	6.28
0.2	0.448	8.34
0.25	0.56	10.36
0.3	0.672	12.35
0.35	0.784	14.28
0.4	0.896	16.13
0.45	1.008	17.86

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.5	1.12	19.45
0.55	1.232	20.85
0.6	1.344	22.03
0.65	1.456	22.98
0.7	1.568	23.67
0.75	1.68	24.11
0.8	1.792	24.29
0.85	1.904	24.24
0.9	2.016	23.99
0.95	2.128	23.6
1	2.24	23.07

revision history

version 1.0 05.30.2007

- initial release of regular versions (CSP2 and COB)
- in table 1-1 on page 1-1, deleted “frame exposure input” from description of pad 03 (FREX) in COB version and pin B4 (FREX) in CSP2 version
- deleted subsection 4.9.2, external processor controlled
- on page 5-13, changed title of subsection 5.11.1 to compression mode 1 timing, moved (previously) figure 5-5 to subsection 5.11.1, re-numbered figure 5-5 to figure 5-1, and re-named it “compression mode 1 timing
- on page 5-14, changed title of subsection 5.11.2 to compression mode 2 timing and re-named figure 5-2 compression mode 2 timing
- deleted previously numbered figures 5-2, 5-3, and 5-4
- in table 5-10 on page 5-15, changed description of register bits DVP_CTRL3D[2:0] (0x363D) to:
  Bit[2:0]: Compression_mode
  000: Mode 2
  001~011: Reserved
  100: Mode 1
  100~111: Reserved
- in table 7-6 on page 7-27, changed description of register bits DVP_CTRL3D[2:0] (0x363D) to:
  Bit[2:0]: Compression_mode
  000: Mode 2
  001~011: Reserved
  100: Mode 1
  100~111: Reserved

version 1.2 10.16.2007

- changed all references of 3.2 Megapixel to 3.1 Megapixel
- under features on page i, removed “CCIR656,” from fifth bullet
- under key specifications on page i, removed “CCIR656,” from fifth bullet
- under key specifications on page i, changed eighth bullet from “**input clock frequency:** 6 ~ 27 MHz” to “**input clock frequency:** 6 ~ 54 MHz”
- in subsection 2.4 on page 2-4, changed first sentence from “The OV3640 PLL allows for an input clock frequency ranging from 6~27 MHz and ...” to “The OV3640 PLL allows for an input clock frequency ranging from 6~54 MHz and ...”
- in subsection 6.1.1 on page 6-1, removed “CCIR656 format,” from first sentence
- in table 6-1 on page 6-1, added “where tp = t_{PCLK}” to timing description for QXGA mode
- in table 6-1 on page 6-2, added “where tp = t_{PCLK}” to timing description for UXGA mode
- in table 6-1 on page 6-2, added “where tp = $t_{PCLK} \times 2$” to timing description for XGA mode
- in table 6-1 on page 6-2, added “where tp = $t_{PCLK} \times 4$” to timing description for SQCIF mode
- in table 7-1 on page 7-1, changed default value for register 0x300B from 0x40 to 0x41 and added “... for REV2a. For REV1a, this register should be 0x40.” to register description

- in table 7-1 on page 7-2, changed description of register bit 0x3012[3] from “CC656 protocol ON/OFF (not used)” to “Reserved”
- in table 7-1 on page 7-6, changed default value of register 0x3021 from 0x0D to 0x1D
- in table 7-1 on page 7-8, changed default values of:
  register 0x307C from 0x00 to 0x10
  register 0x307D from 0x00 to 0x20
- in table 7-1 on page 7-9, changed default values of:
  register 0x30B0 from 0xFF to 0x00
  register 0x30B1 from 0xEF to 0x00
- in table 7-2 on page 7-9, changed default values of:
- register 0x3400 from 0x04 to 0x03
- register 0x3403 from 0x00 to 0x42
- in table 7-2 on page 7-10, changed default value of register 0x3404 from 0x02 to 0x18
- in table 8-3 on page 8-3, changed parameter in sixth row from “setting time for UXGA/SVGA mode change” to “setting time for QXGA/XGA mode change”
- in table 8-3 on page 8-3, removed rows for digital inputs, digital outputs and serial interface inputs
- in table 8-4 on page 8-3, changed max value for frequency (XVCLK) from “27” to “54”

version 1.3 **12.12.2007**

- under key specifications on page i, changed active power requirements to “75 mA (without MIPI)”, standby power requirements to “20µA”, sensitivity to “490 mV/(Lux • sec)”, S/N ratio to “36 dB”, dynamic range to “60 dB”, well capacity to “72 Ke^-”, dark current to “<3 mV/s @ 60°C”, and fixed pattern noise (FPN) to “1% of $V_{PEAK-TO-PEAK}$”
- on page 2-2, replaced figure 2-2 with updated reference design schematic
- in table 4-2 on page 4-2, added footnote a to vertical start function on second row
- in table 7-1 on page7-1, changed registers 0x3005, 0x3006, and 0x3007 to RSVD
- in table 7-1 on page 7-14, changed register name, default value, and R/W type of register 0x30A9 to “PWCOM1”, “0xB5”, and “RW”, respectively
- in table 7-1 on page 14, changed description of register 0x30A9 to:
  Power Common Control 1
  Bit[7:4]: Reserved
  Bit[3]: Bypass regulator
  Bit[2:0]: Reserved
- in table 8-2 on page 8-2, changed original footnote a to footnote d
- in table 8-2 on page 8-2, changed max value of V_{DD-IO} from “3.0” to “1.89”
- in table 8-2 on page 8-2, added footnote a, “using the internal DVDD regulator is strongly recommended for minimum power down current”, footnote b, “active current is based on sensor resolution at full size and at full speed in compression format”, and footnote c, “with the MIPI function, the active current needs an additional 20 mA”
- in table 8-2 on page 8-2, deleted TBDs for min values of active (operating) current and standby current and deleted row for I_{DD-D}
- in table 8-2 on page 8-2, changed typ values of active (operating) current and standby current to “35” for I_{DD-A}, “75” for I_{DD-IO}, “20” for $I_{DDS-SCCB}$, and “20” for $I_{DDS-PWDN}$
- in table 8-2 on page 8-2, changed max values of active (operating) current and standby current to “40” for I_{DD-A}, “110” for I_{DD-IO}, “40” for $I_{DDS-SCCB}$, and “40” for $I_{DDS-PWDN}$

version 1.4 01.11.2008

- under key specifications on page i, changed I/O power supply requirements from “1.8VDC ± 5%” to “1.7 ~ 3.0V (1.8V is strongly recommended)”
- in Table 8-2 on page 8-2, changed min, typ, and max for supply voltage (digital I/O) V_{DD-IO} from “1.71”, “1.8”, and “1.89” to “1.7”, “1.8”, and “3.0”, respectively
- in table 8-2 on page 8-2, changed unit for standby current ($I_{DDS-SCCB}$) from “mA” to “µA”
- in table 8-2 on page 8-2, changed max for SCL and SDA (V_{IH}) from “2.3” to “3.0”

version 1.5 02.19.2008

- in section 8 on page 8-4, added figure 8-1, SCCB interface timing
- in section 8 on page 8-4, added table 8-5, SCCB interface timing specifications
- in section 8 on page 8-5, added figure 8-2, line/pixel output timing
- in section 8 on page 8-5, added table 8-6, pixel timing specifications

version 2.0 03.21.2008

- changed document from Preliminary Specification to Product Specification
- in section 8 on page 8-1, deleted row for “ambient humidity” from table 8-1, absolute maximum ratings
- in section 8 on page 8-2, added footnote e, “at room temperature and typical supply voltages,” to $I_{DDS-SCCB}$ and $I_{DDS-PWDN}$ in table 8-2, DC characteristics (-20°C < T_A < 70°C)

version 2.1 09.25.2008

- in figure 2-2 on page 2-2, added note 3 to schematic
- made major changes to subsection 2.4, power up sequence including adding figures 2-3 to 2-6
- in table 8-2 on page 8-2, changed max spec for active (operating) current (IDD-A) from "40" to "50" and added footnote c, “maximum in-rush current on AVDD is 100 mA
- in table 8-2 on page 8-2, changed typ and max specs for active (operating) current (IDD-IO) from "75" and "110" to "95" and "125," respectively and added footnote f, “maximum in-rush current on DOVDD is 200 mA
- in subsection 2.5 on page 2-9, added second paragraph
- in subsection 2.6 on page 2-9, added “To avoid an in-rush of current on AVDD, power down the analog circuit by setting register 0x300E[7] to 1’b1 before pulling PWDN to high. For wakeup, after releasing PWDN pin from high to low, un-power down the analog circuit by setting register 0x300E[7] to 1’b0 to resume video.”

version 2.2 10.07.2008

- added items 5 and 6 to subsection 2.4.1, items 4 and 5 to subsection 2.4.2, items 6 and 7 to subsection 2.4.3, and items 4 and 5 to subsection 2.4.4
- added subsections 2.6.1, 2.6.1.1, 2.6.1.2 and 2.6.2 on pages 2-9 and 2-10 describing hardware standby, software sleep and return to normal mode procedures from either hardware standby and software sleep modes
- in table 7-1, changed description of register bit 0x3086[3] to Wakeup reset enable

version 2.21 10.14.2008

- in table 8-2, added rows for active (operating) power consumption (P_O) and standby power consumption ($P_{DDS-SCCB}$ and $P_{DDS-PWDN}$)
- in table 8-2, added footnote g, "active power consumption value is 1.8V V_{DD-IO}

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